

GA-A320M-HD2

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[illegible]

Version: 1.0

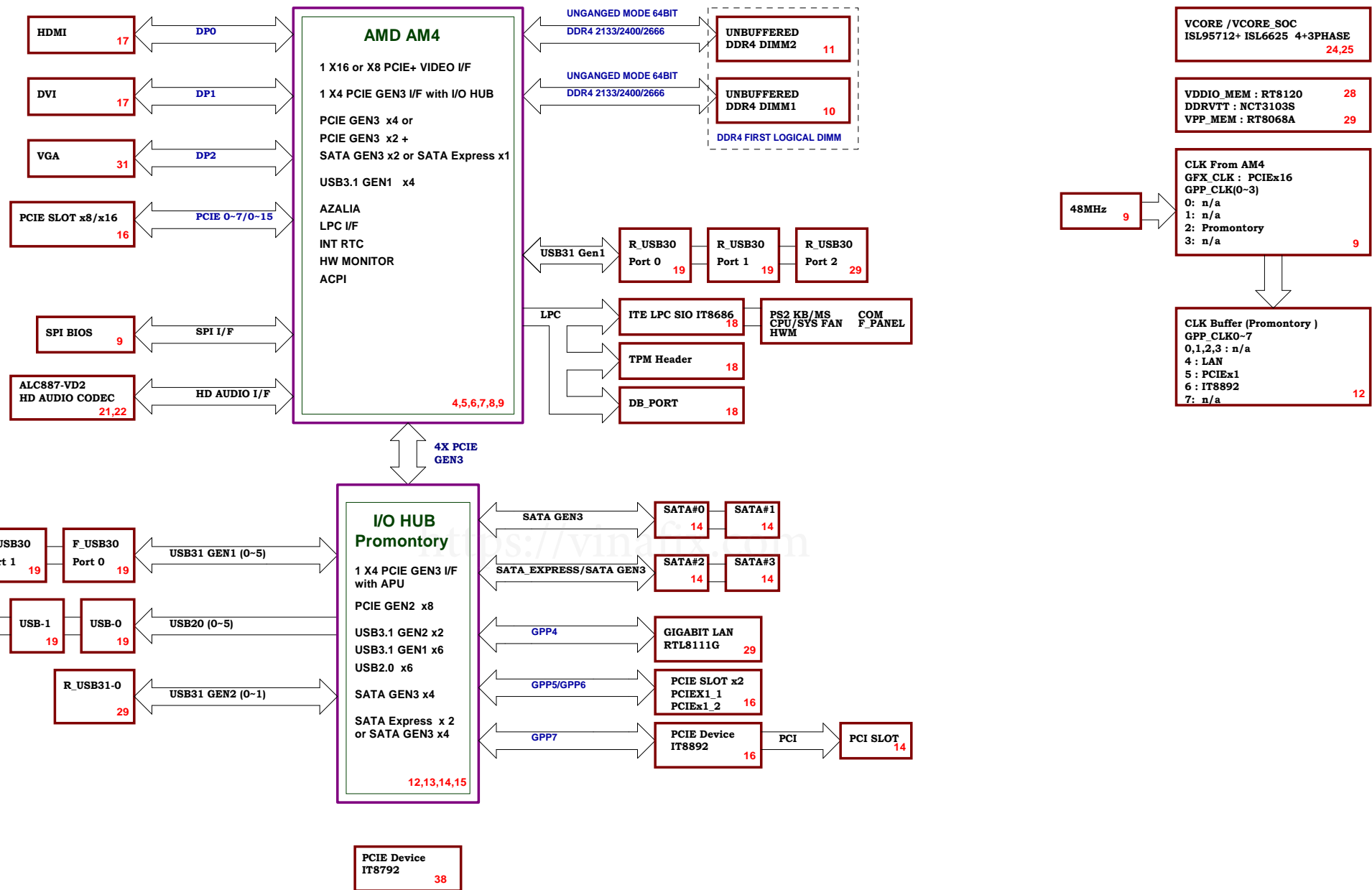
Component value change history

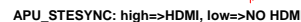
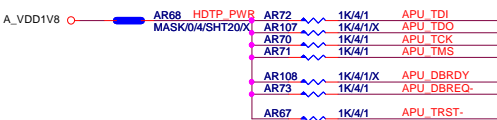
**P-Code: U16141-0
9MA32MHD2-00**

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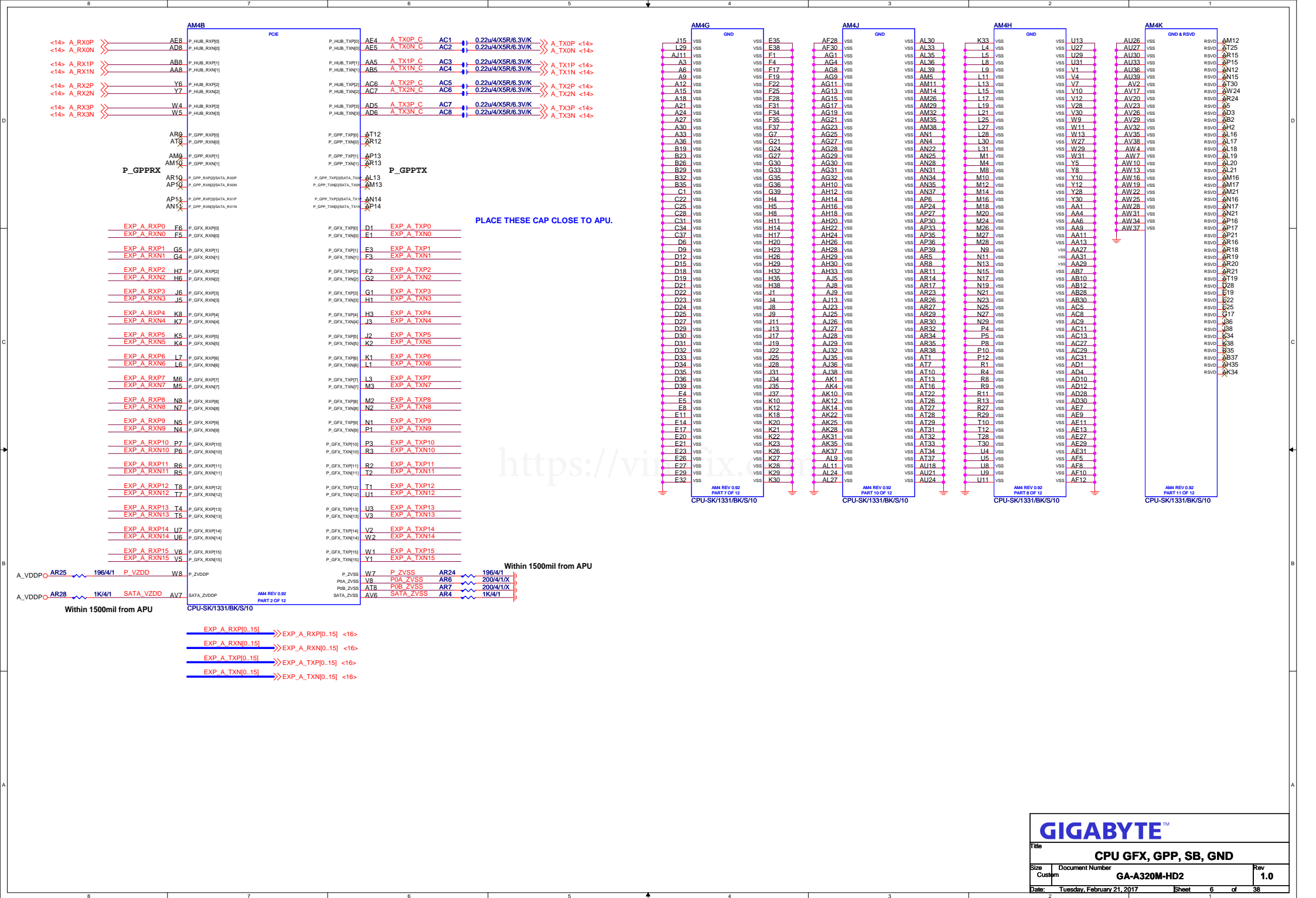
Circuit or PCB layout change for next version

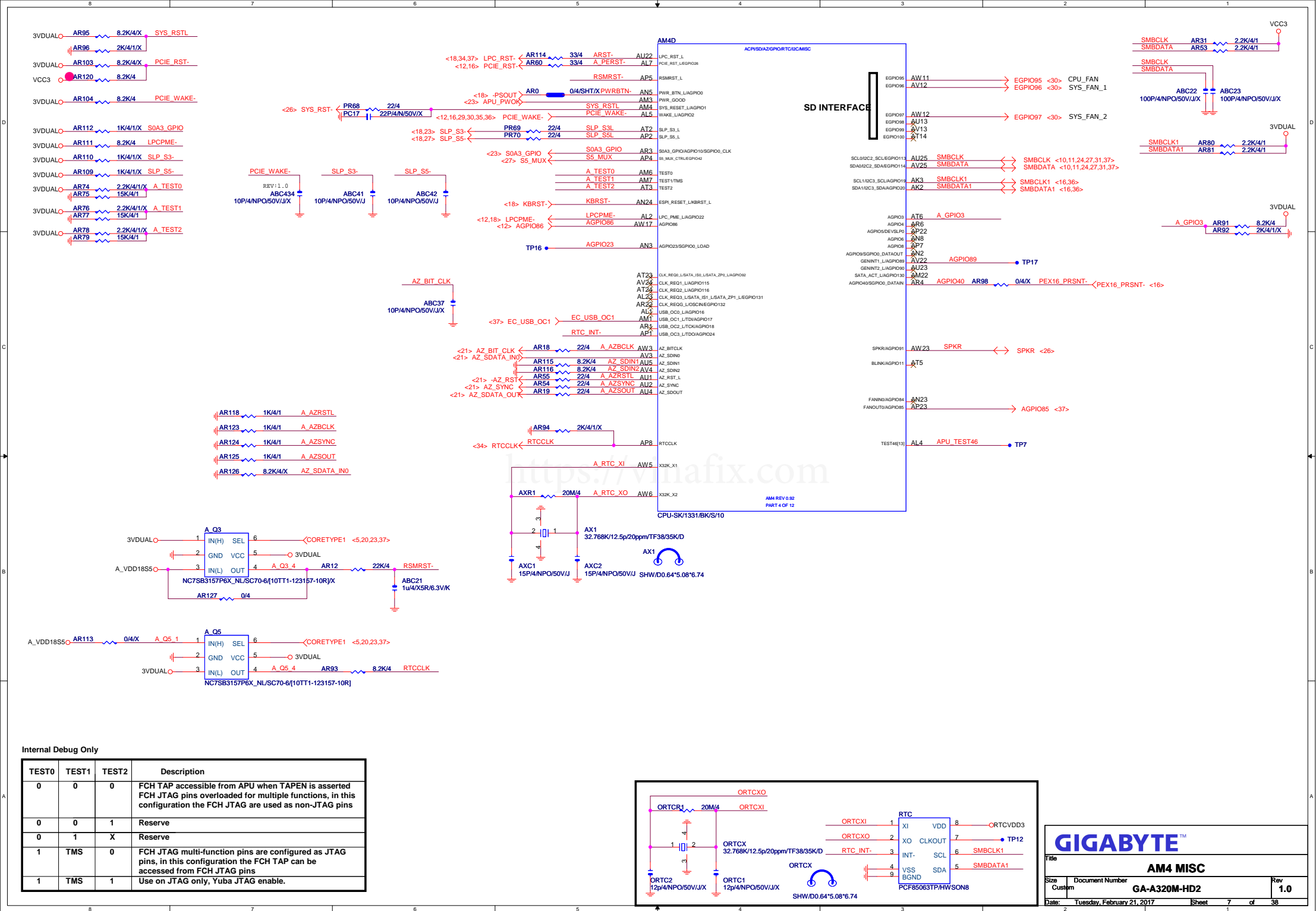
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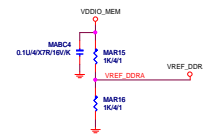
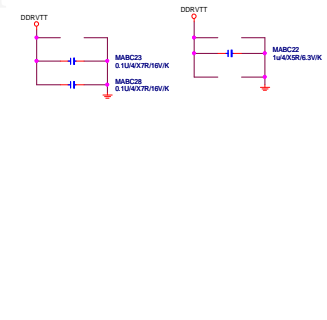
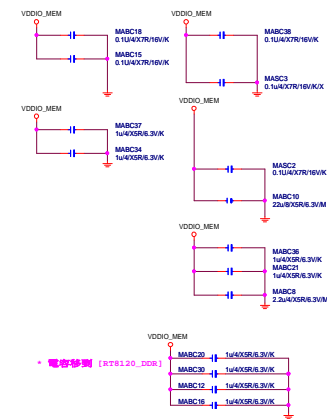
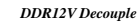
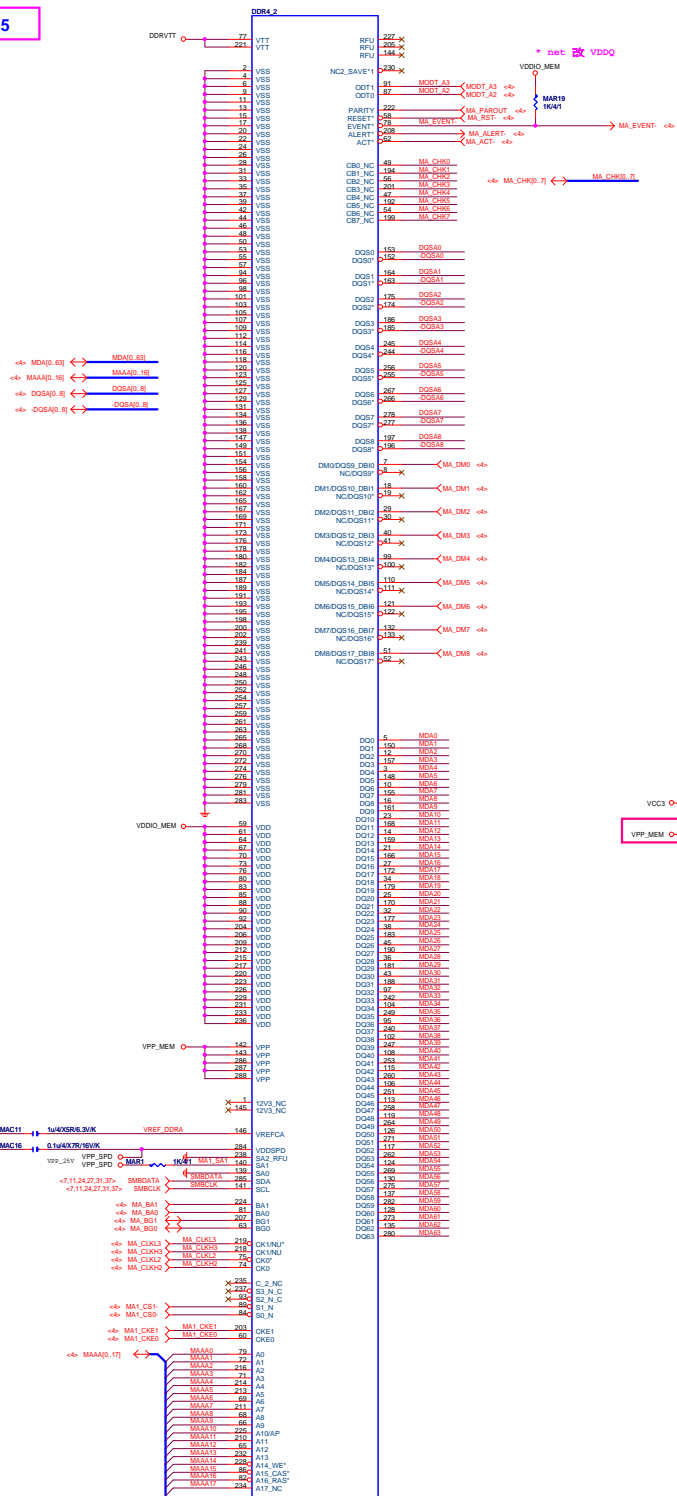


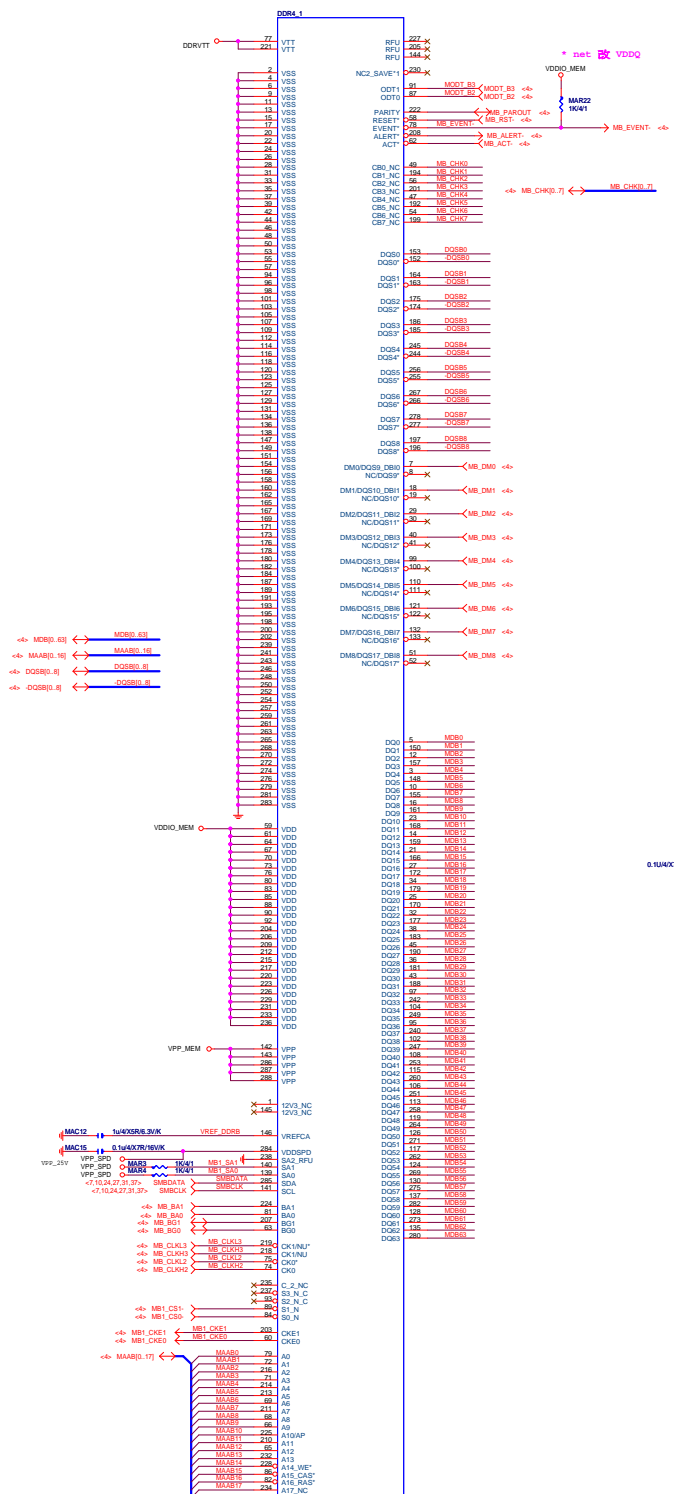
Title			
CPU DDI, CONTROL			
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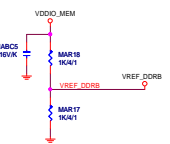


Rev:0.5



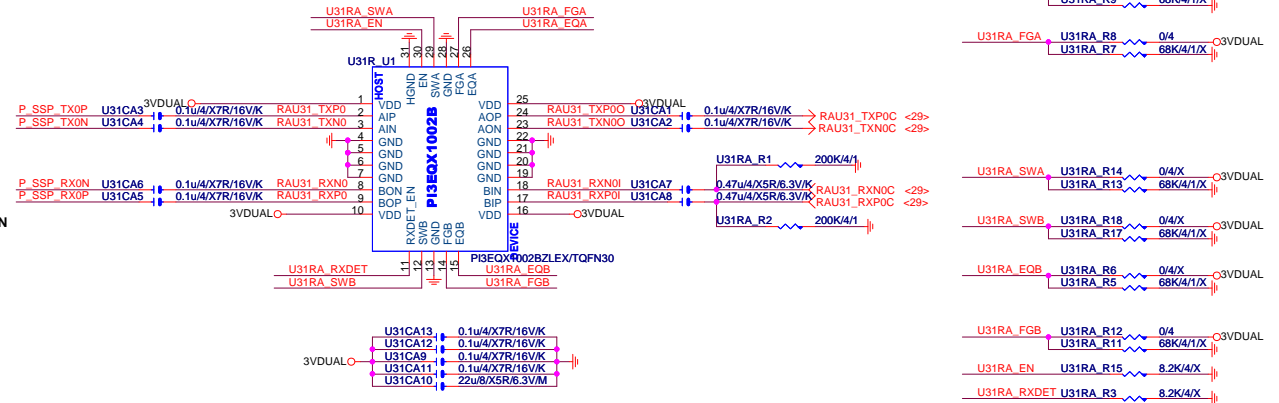
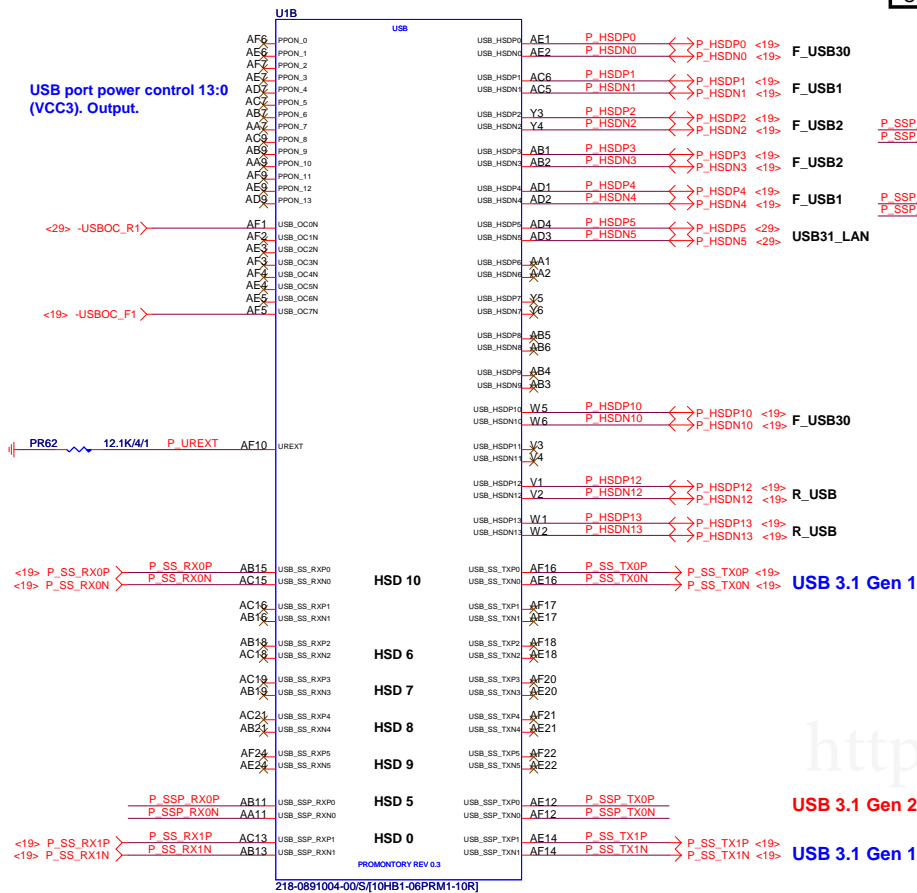


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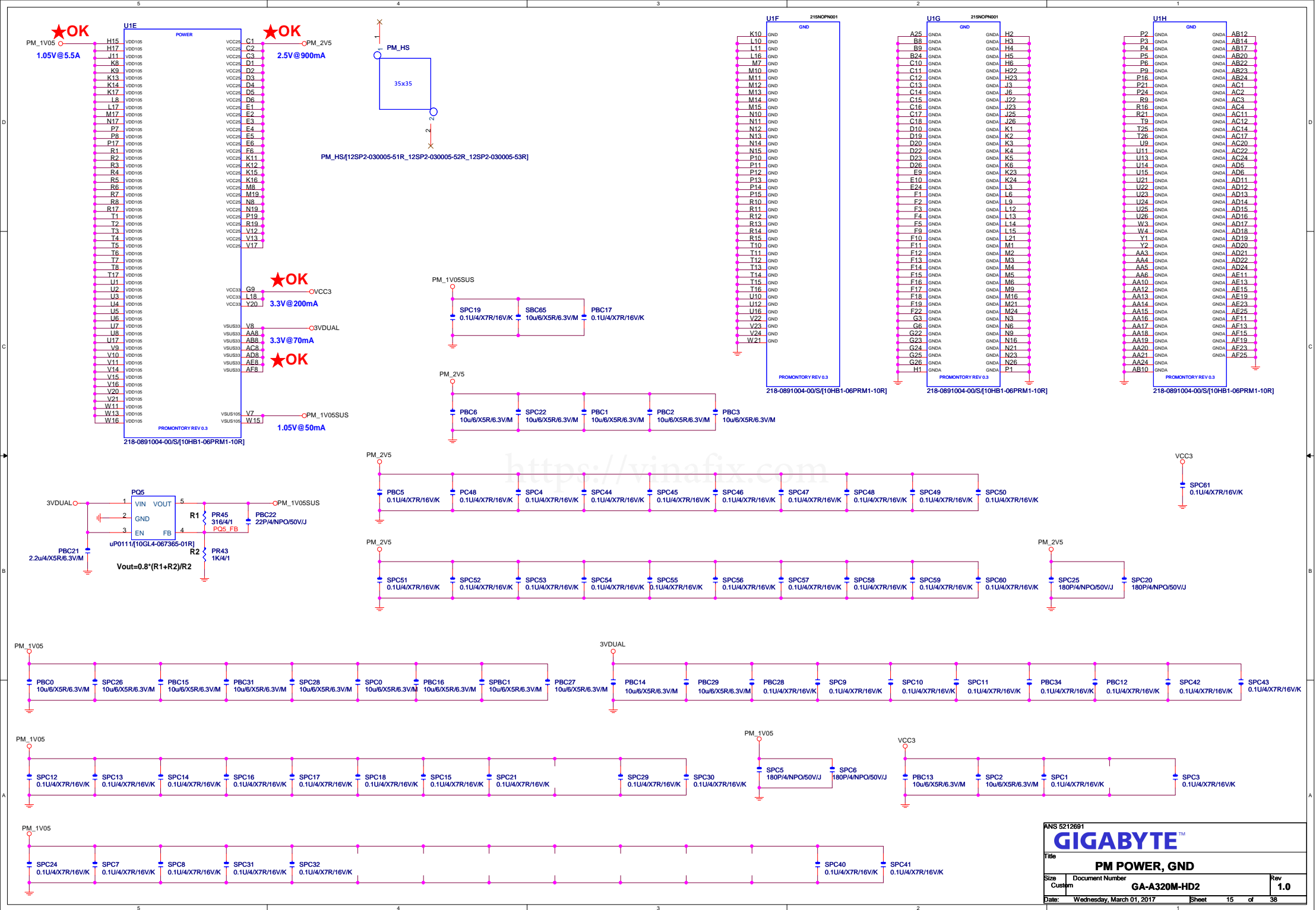
CHANNEL B1
SA2:3=011

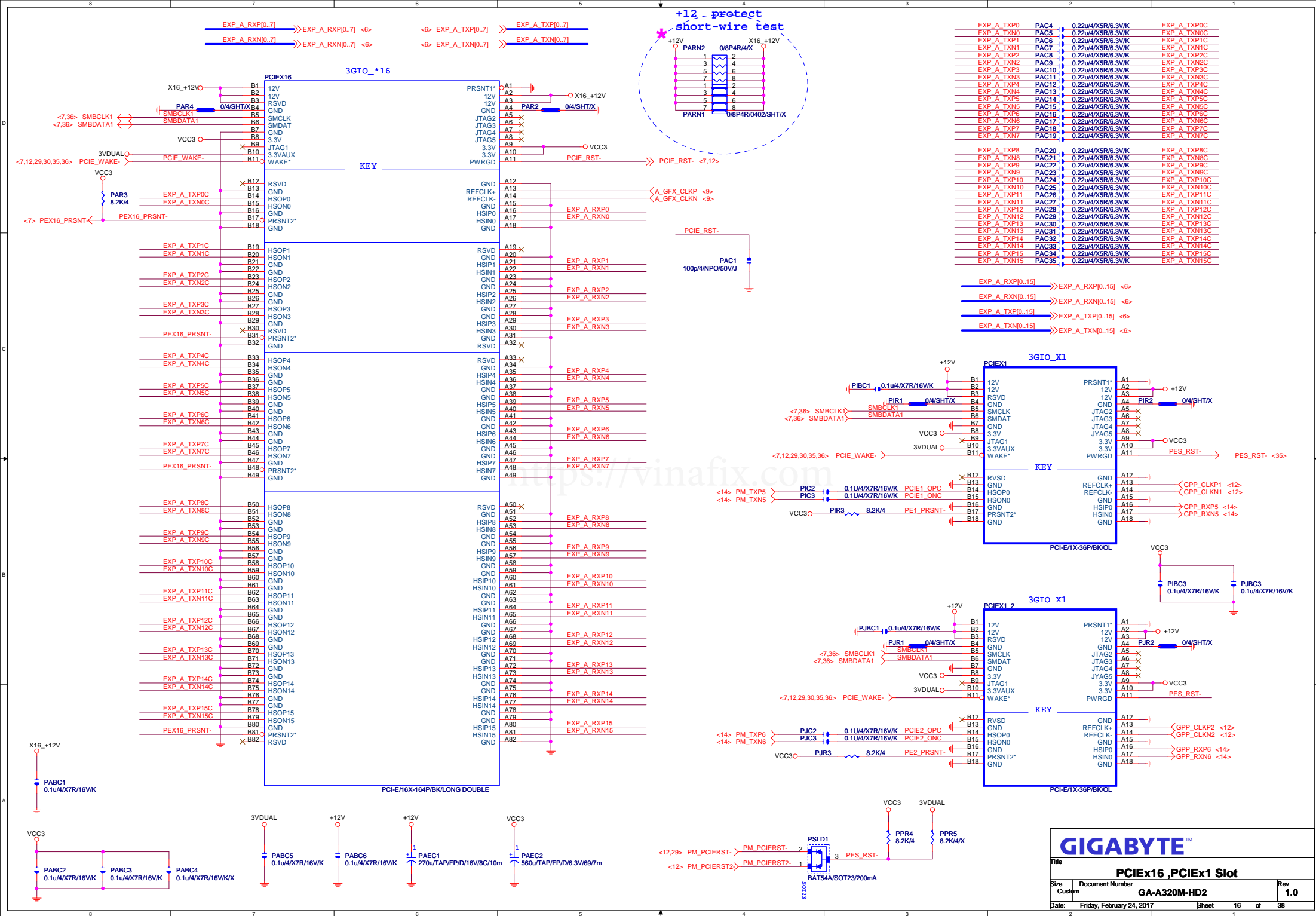
USB3.1 Re-Driver



USB3.1	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0





PWR	SHT
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For 8728 EUP function

3VDUAL_IO OR25 0/6/SHT/X IT_VCC

VCC3 OR8 0/4/SHT/20/X IT_AVCC

VCC3 ○ — OR16 — 8.2K/4 — SIO_WD
— OR24 — 8.2K/4 — -PCIE_RST

THROM SPARE GPIO

SIO STRAP

JP2 OR36 8.2K/4

OR33 1K/4/1/A JP3 OR35 8.2K/4/X 3VDDUAL_IO
OR81 1K/4/1/X JP4 OR32 8.2K/4 3VDDUAL_IO
OR80 1K/4/1/X JP5 OR12 8.2K/4 3VDDUAL_IO
JP7 CN_N2 OR37 8.2K/4 3VDDUAL_IO

SIO PU

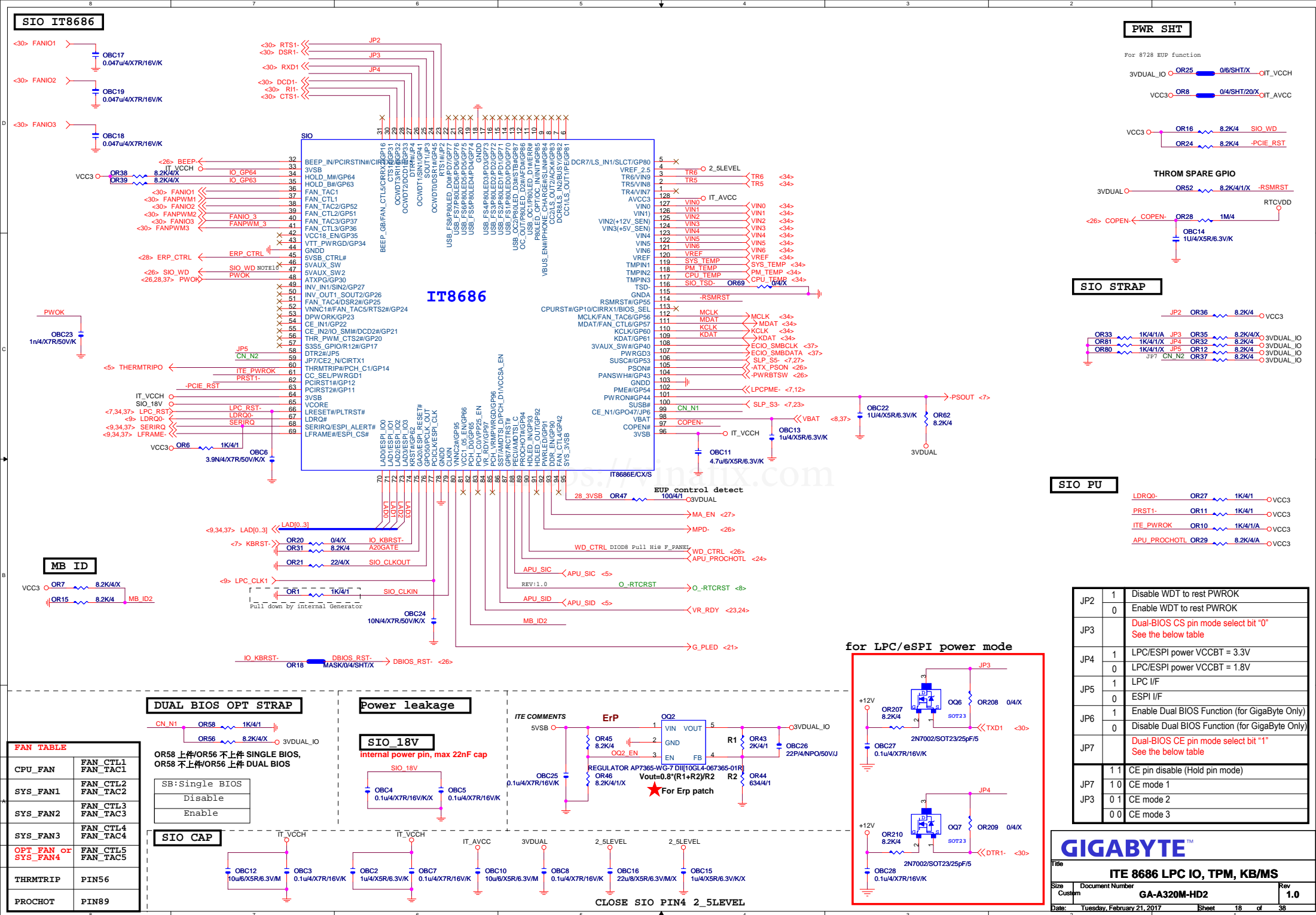
LDRQ0- OR27 1K/4/1 VCC3
 PRST1- OR11 1K/4/1 VCC3
 ITE_PWROK OR10 1K/4/1/A VCC3
 APU_PROCHOTL OR29 8.2K/4/A VCC3

JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7 JP3	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
	0 1	CE mode 2
	0 0	CE mode 3

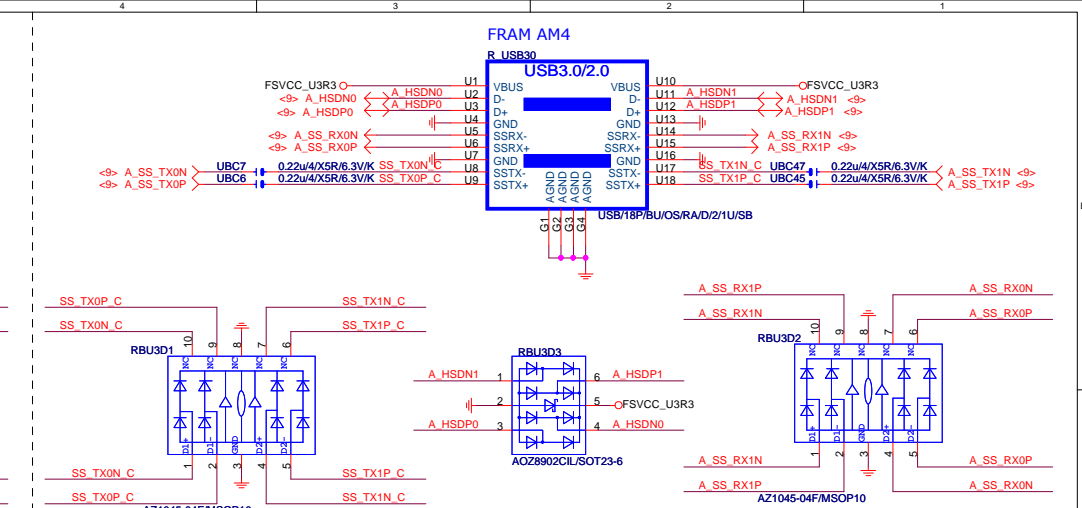
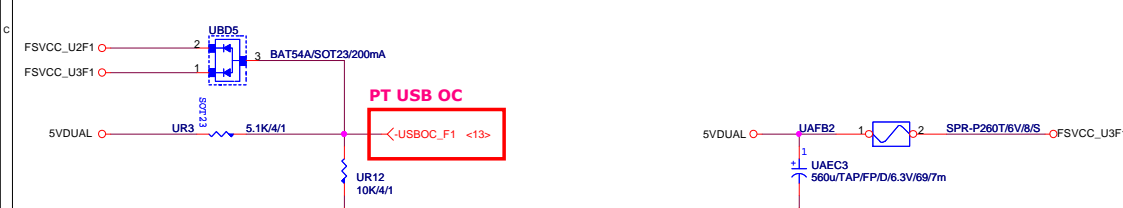
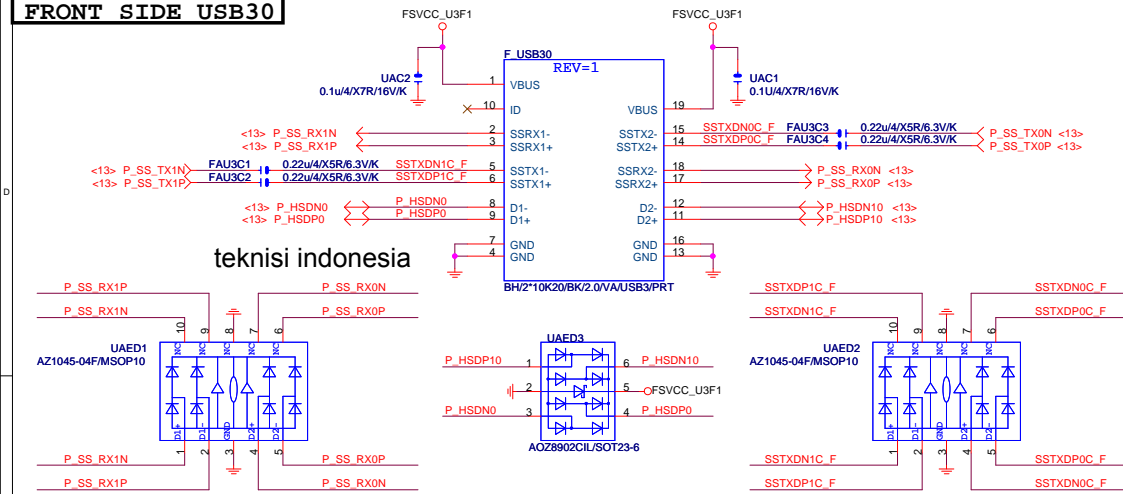
GIGABYTE™

ITE 8686 LPC IO, TPM, KB/MS

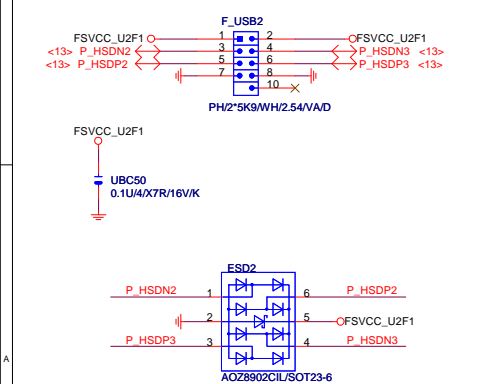
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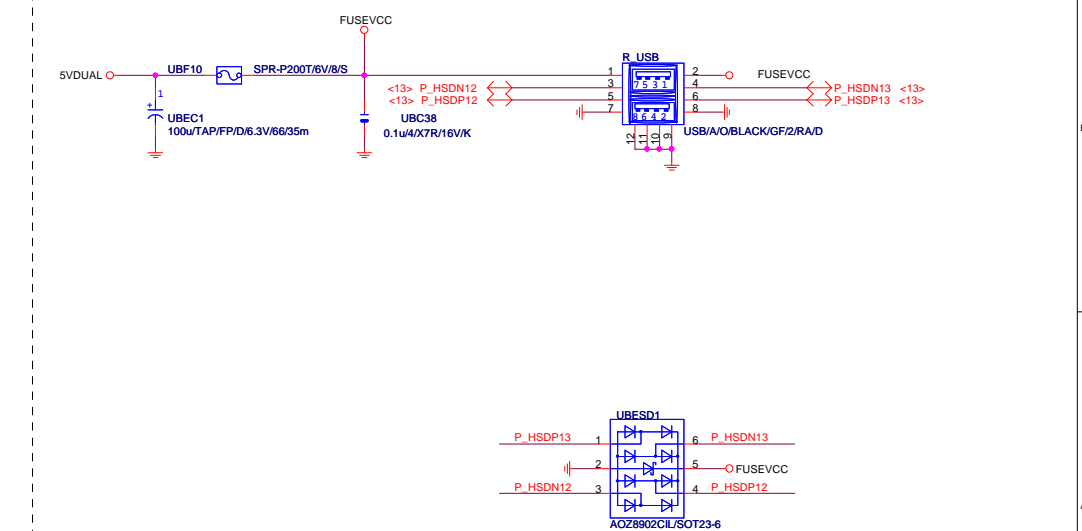
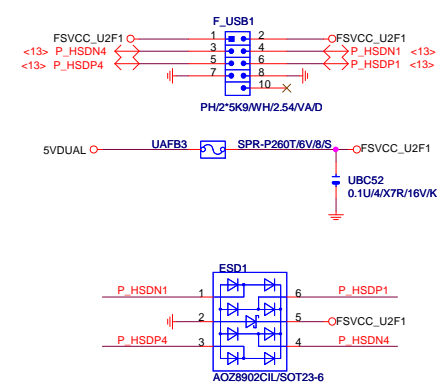
FRONT SIDE USB30



FRONT SIDE USB2

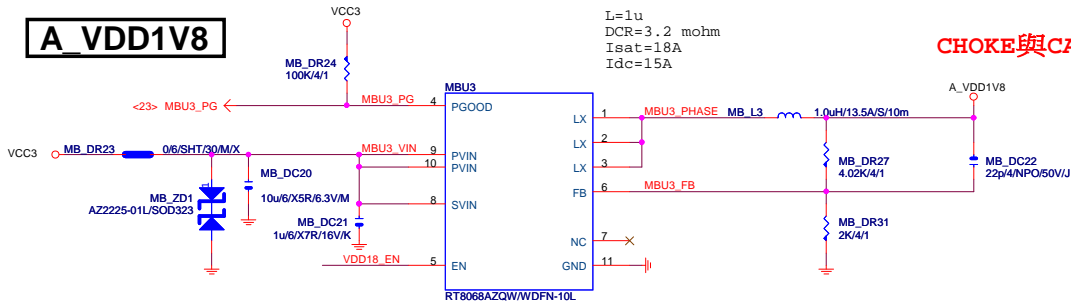


FRONT SIDE USB1



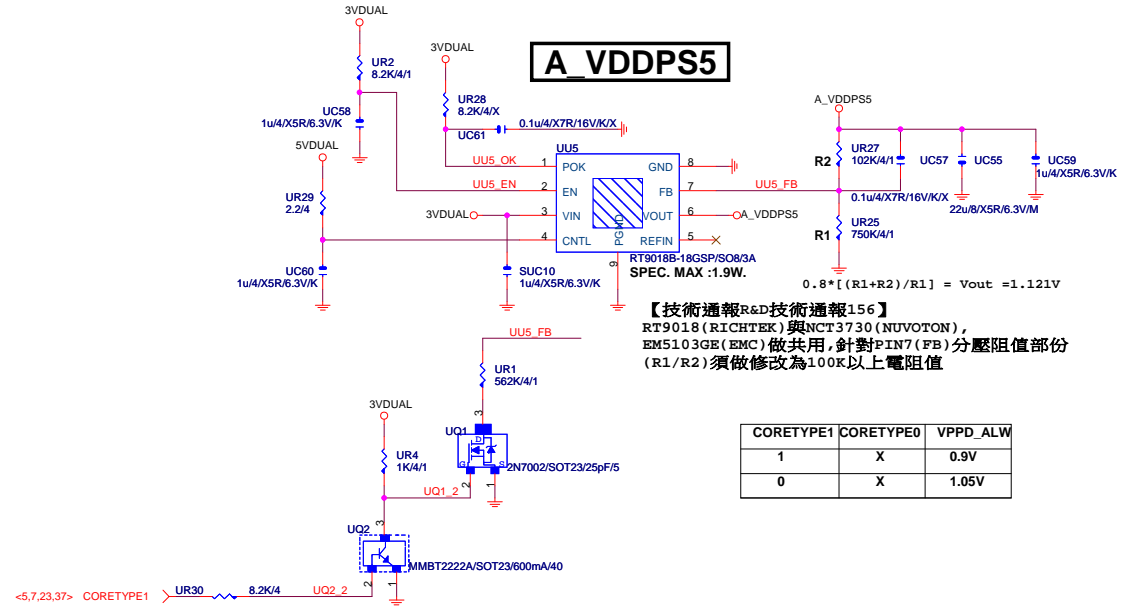
REV:0.4

A_VDD1V8



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A_VDDPS5



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

PWR_SEQ

* 刪 MA_DR32

VPP CAP

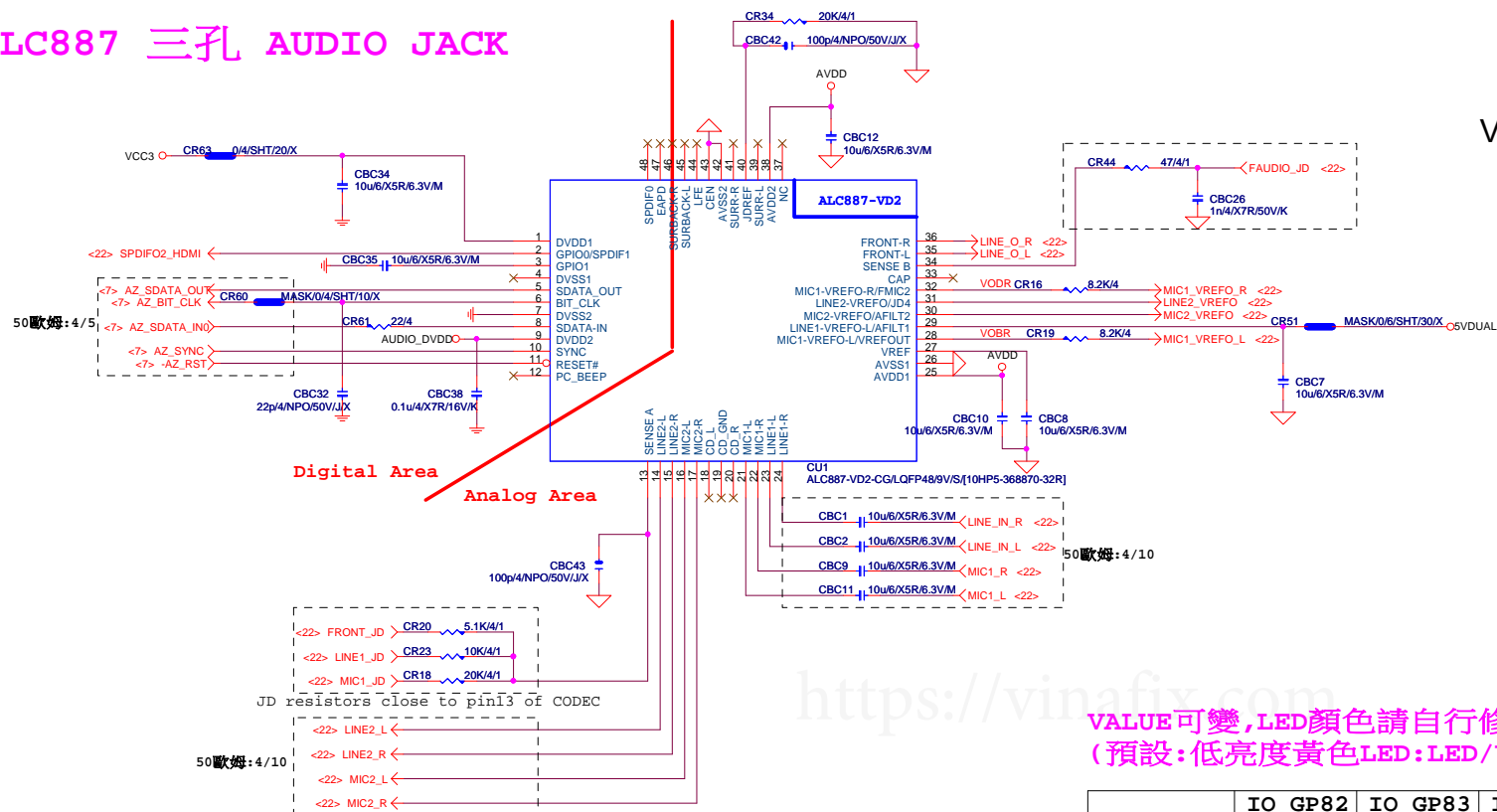
* 大電容 ∞0

22u*1PCS

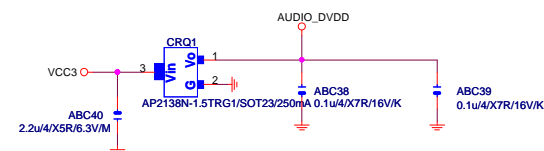
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Title	A_VDD1V8, A_VDDPS5	
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ALC887 三孔 AUDIO JACK



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LAYOUT注意: 螺絲孔下GND方式

- MH1空間夠, 下DGND
空間不夠, 改為Isolate
- MH2一律改為Isolate

VALUE可變, LED顏色請自行修改
(預設: 低亮度黃色LED: LED/Y/6/S)

	IO_GP82	IO_GP83	IO_GP91
LED	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH

<input type="radio"/> MH1	<input type="radio"/> MH2
DGND	Isolate

LAYOUT注意: 要加

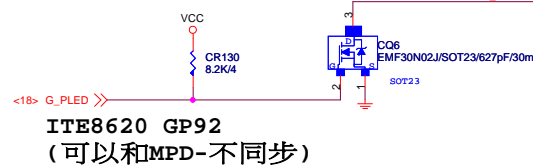
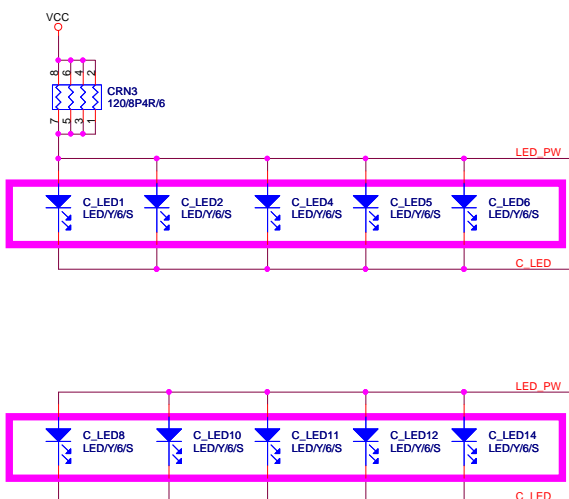
GND切割線

音效區域印刷



GIGABYTE		
Title: ALC887 CODEC		
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AUDIO LED Control (沒有LPT model)

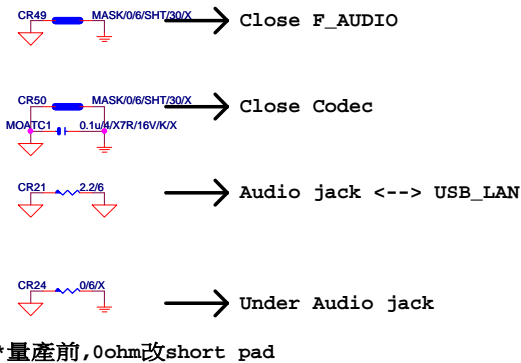


ITE8620 GP92
(可以和MPD-不同步)

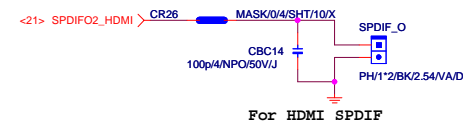
BOM OPTION :

- Chemicon 音效電容
- 金屬外罩 Reserve (上件與否, 依照各Model spec)
- LED Reserve (上件與否和LED顏色, 依照各Model spec)

Rev 0.5

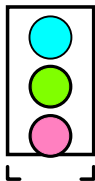


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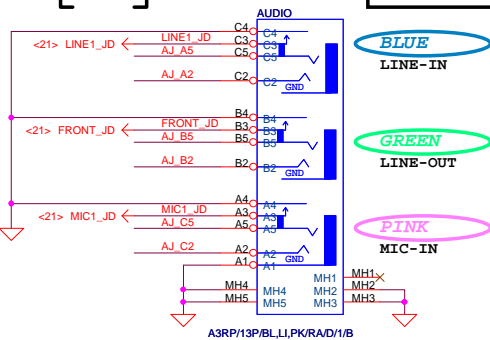


SPDIF_IN

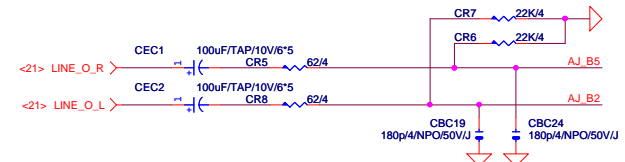
AZALIA JACK



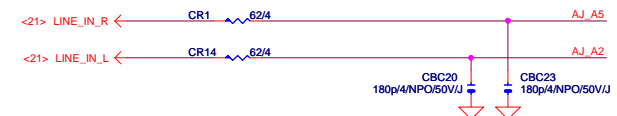
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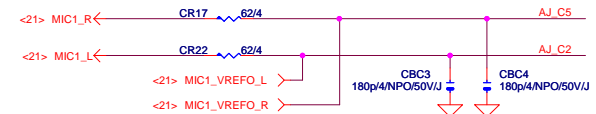
LINE-OUT



LINE-IN



MIC-IN

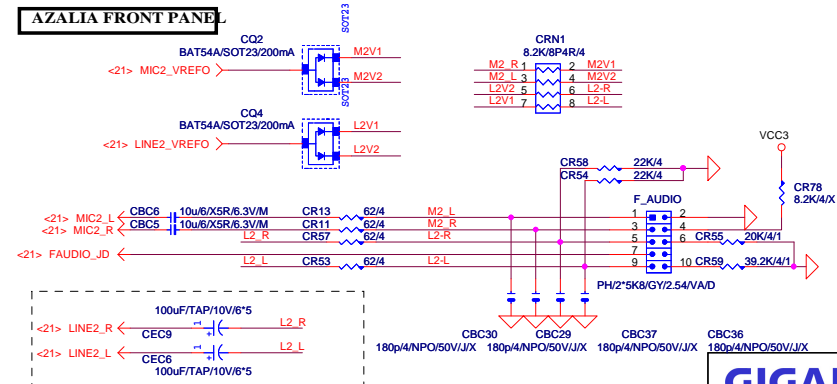


SURROUND

CEN/LFE

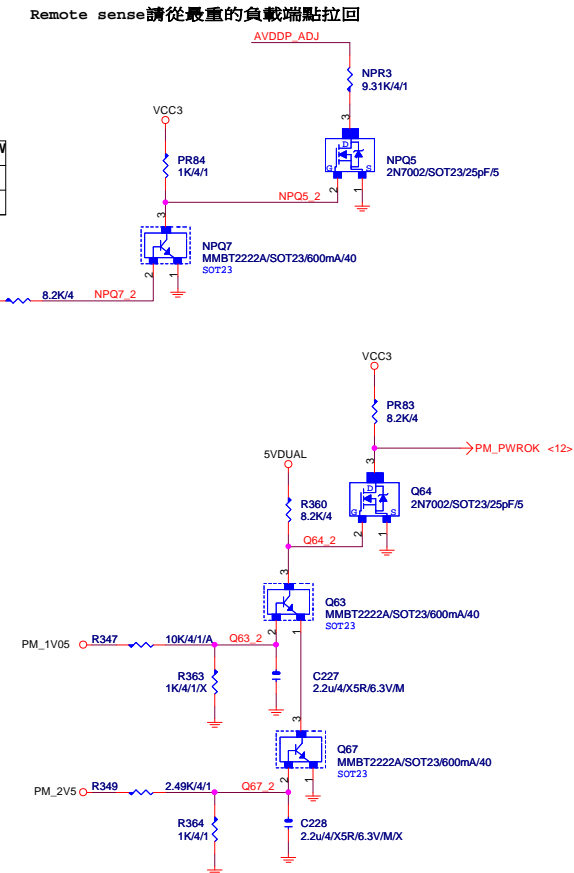
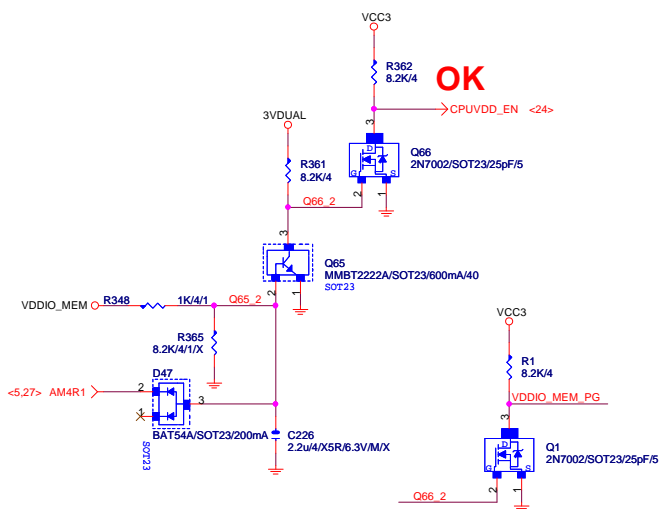
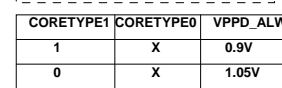
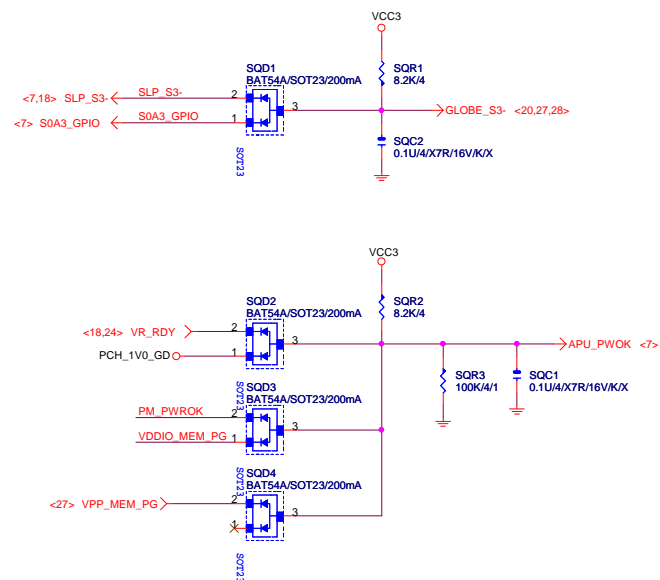
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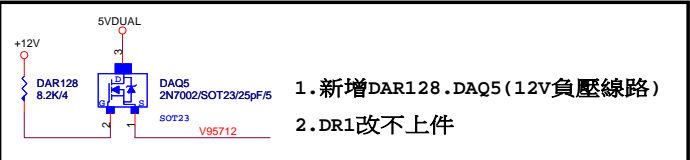
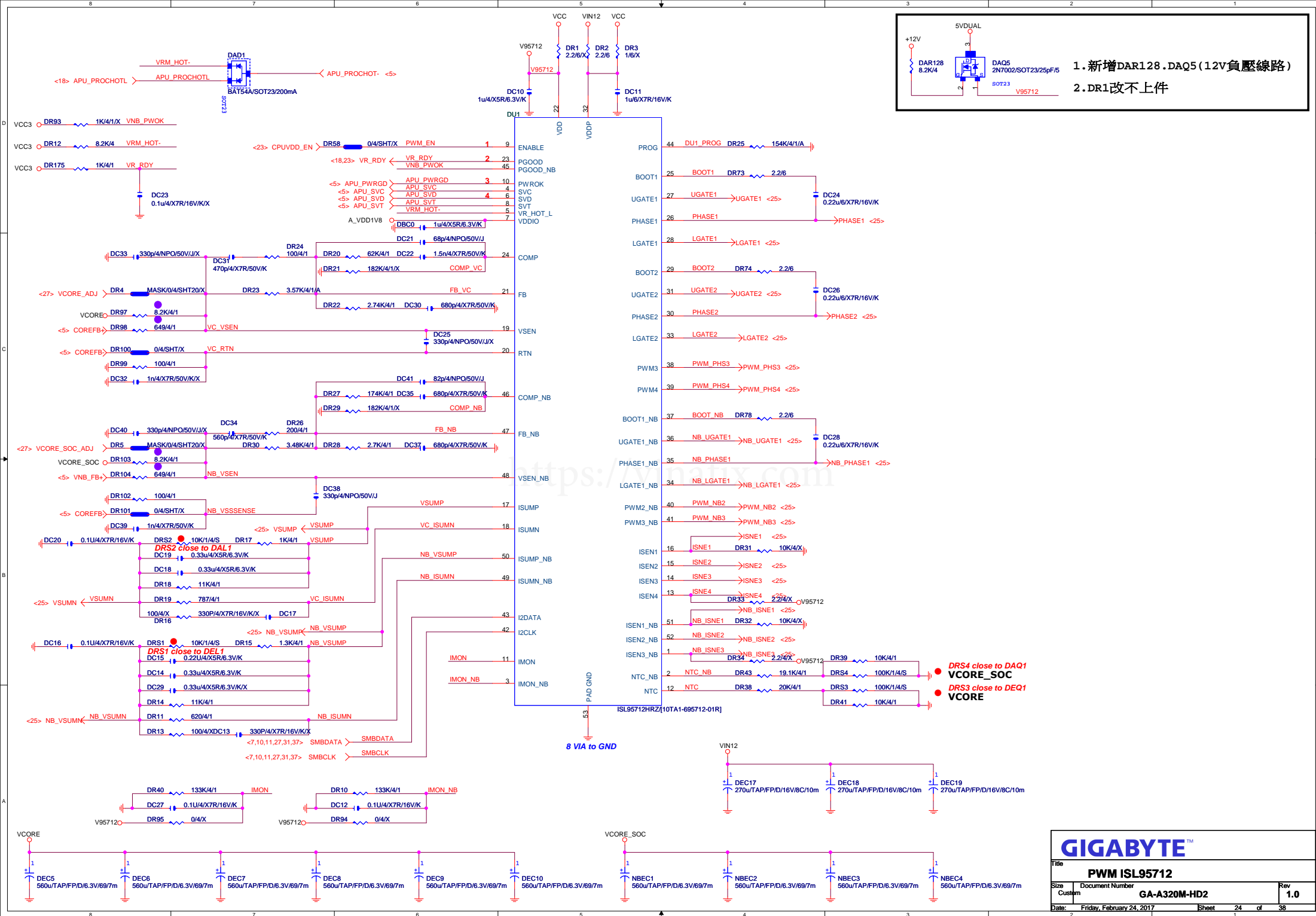
AZALIA FRONT PANEL



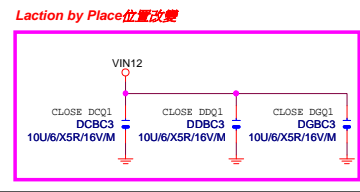
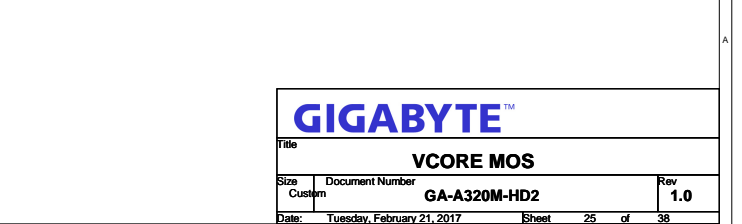
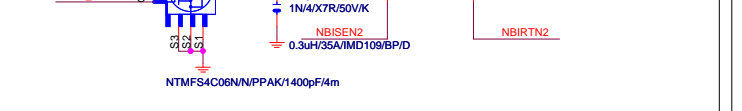
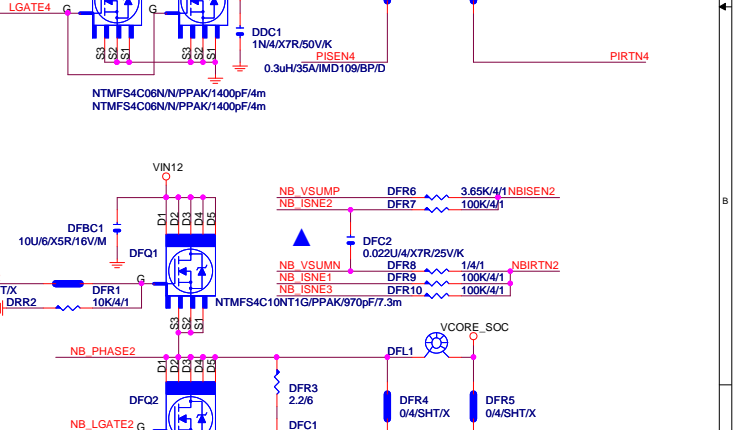
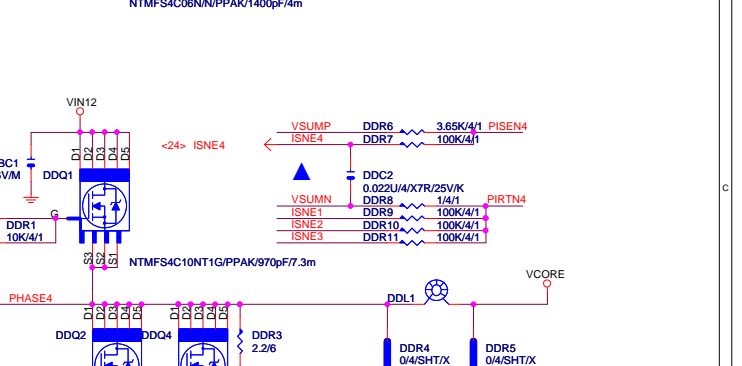
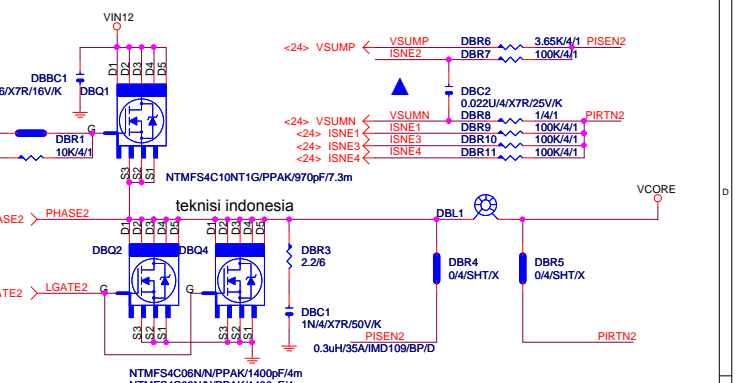
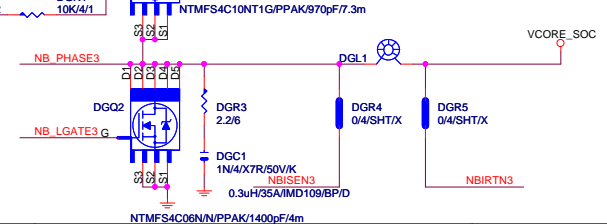
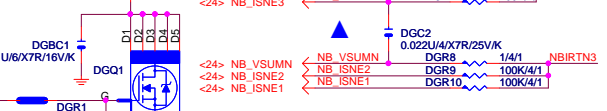
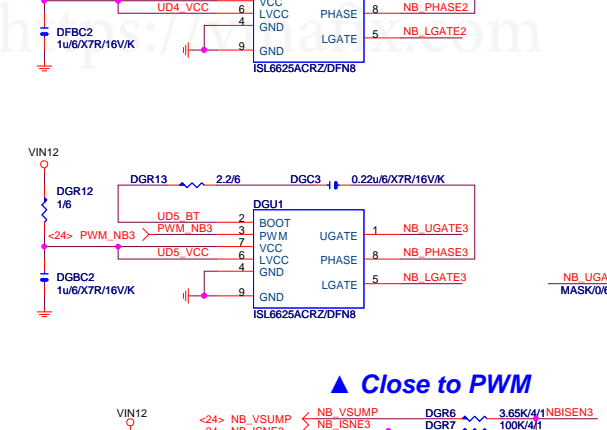
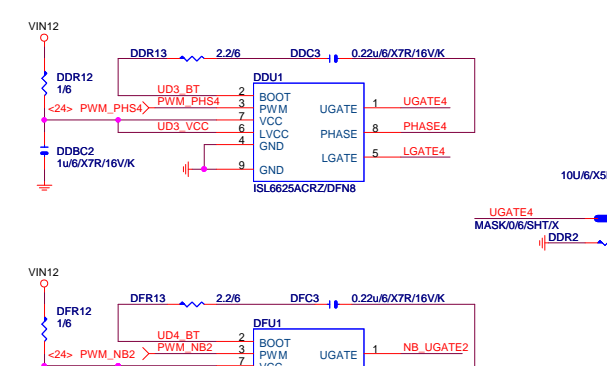
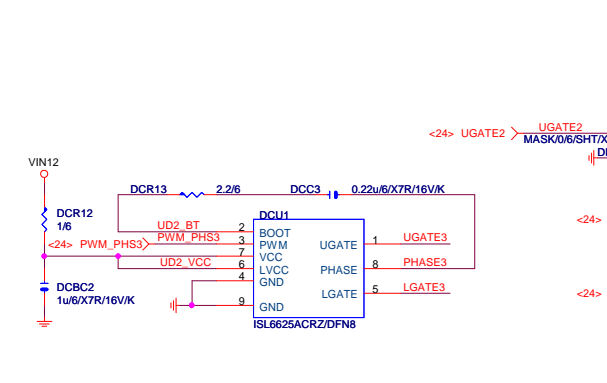
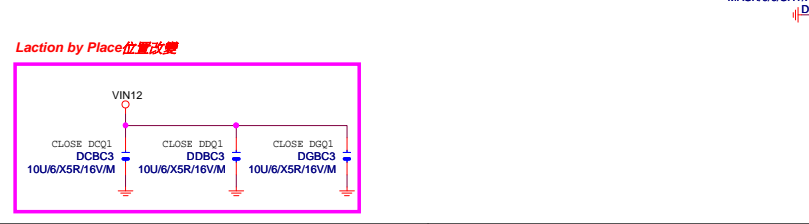
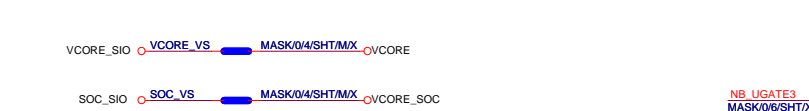
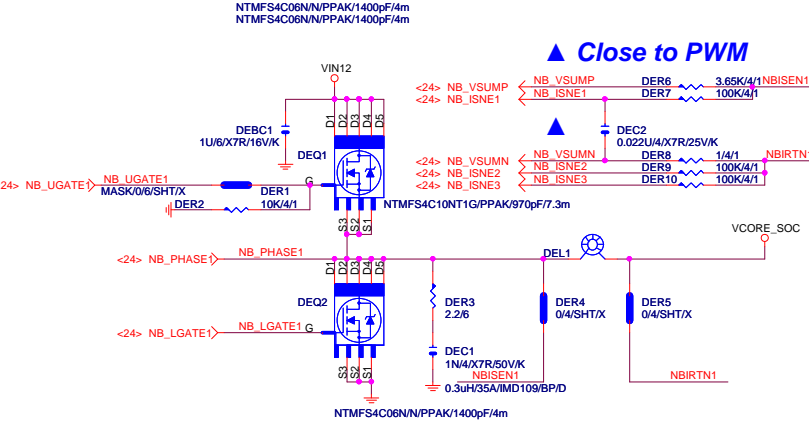
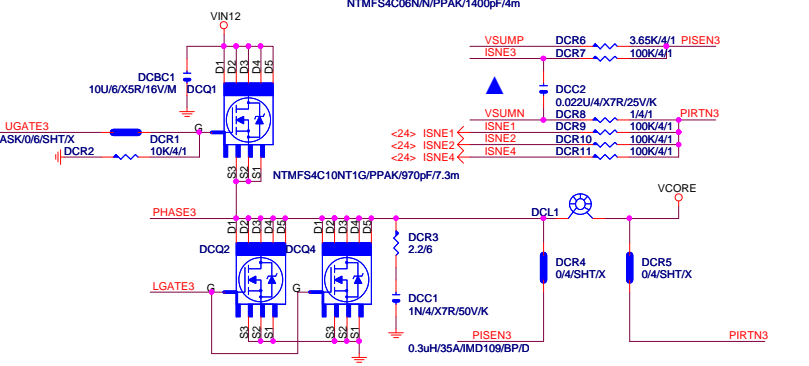
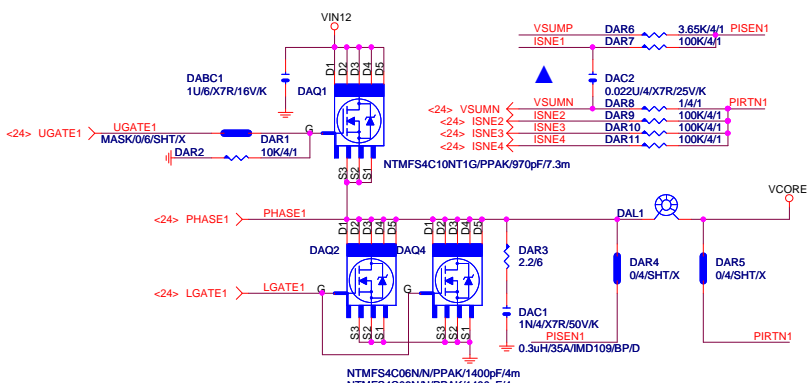
GIGABYTE™

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AUDIO JACK		
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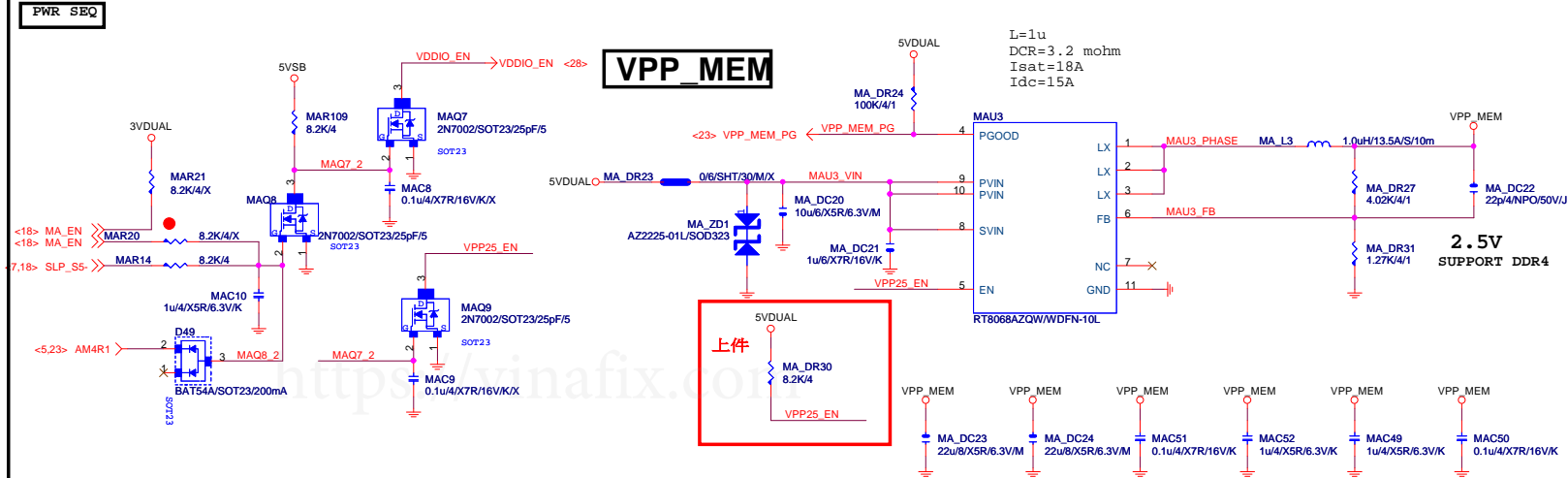
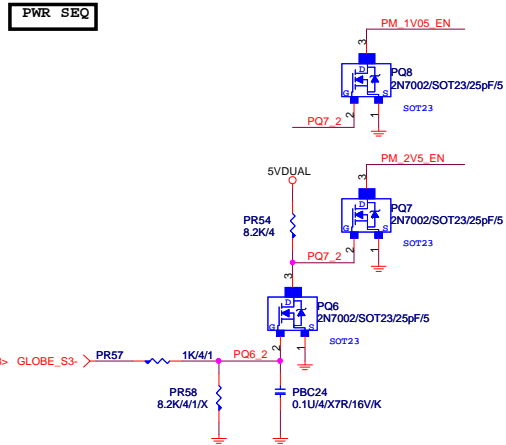
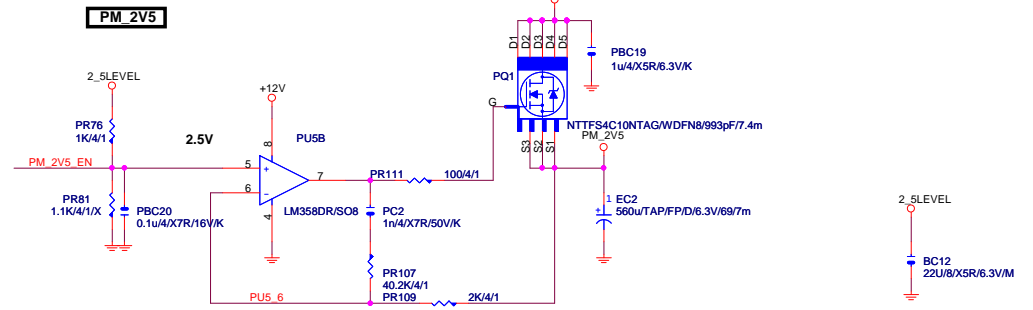
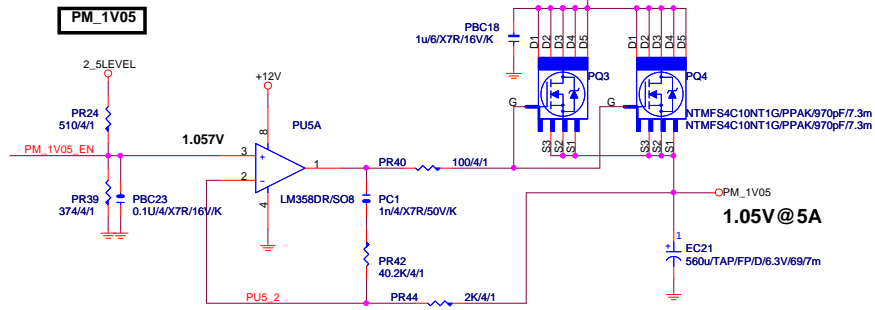




- 1. 新增DAR128.DAQ5 (12V負壓線路)
- 2. DR1改不上件

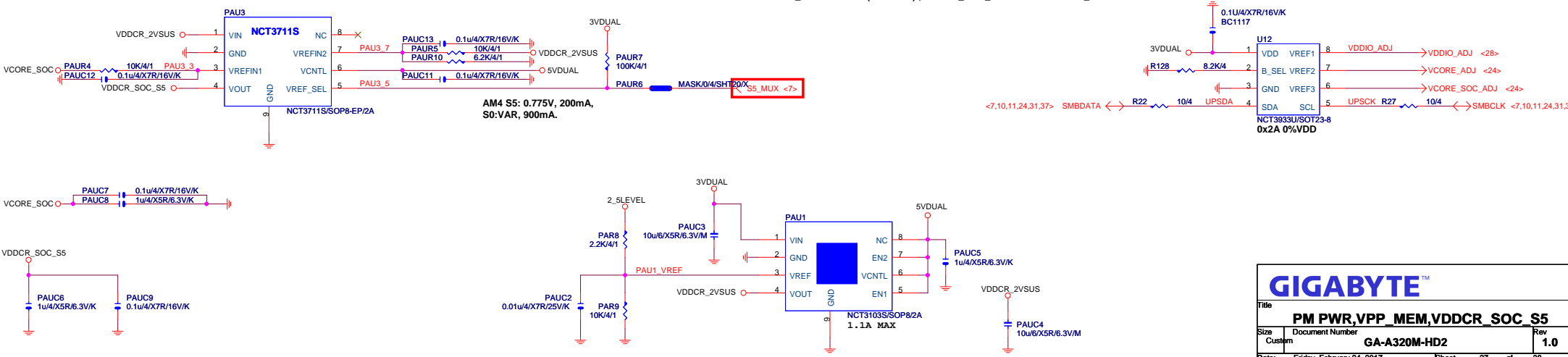


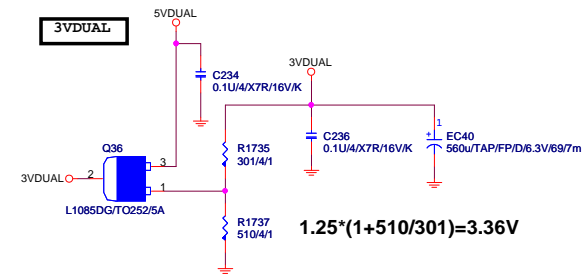
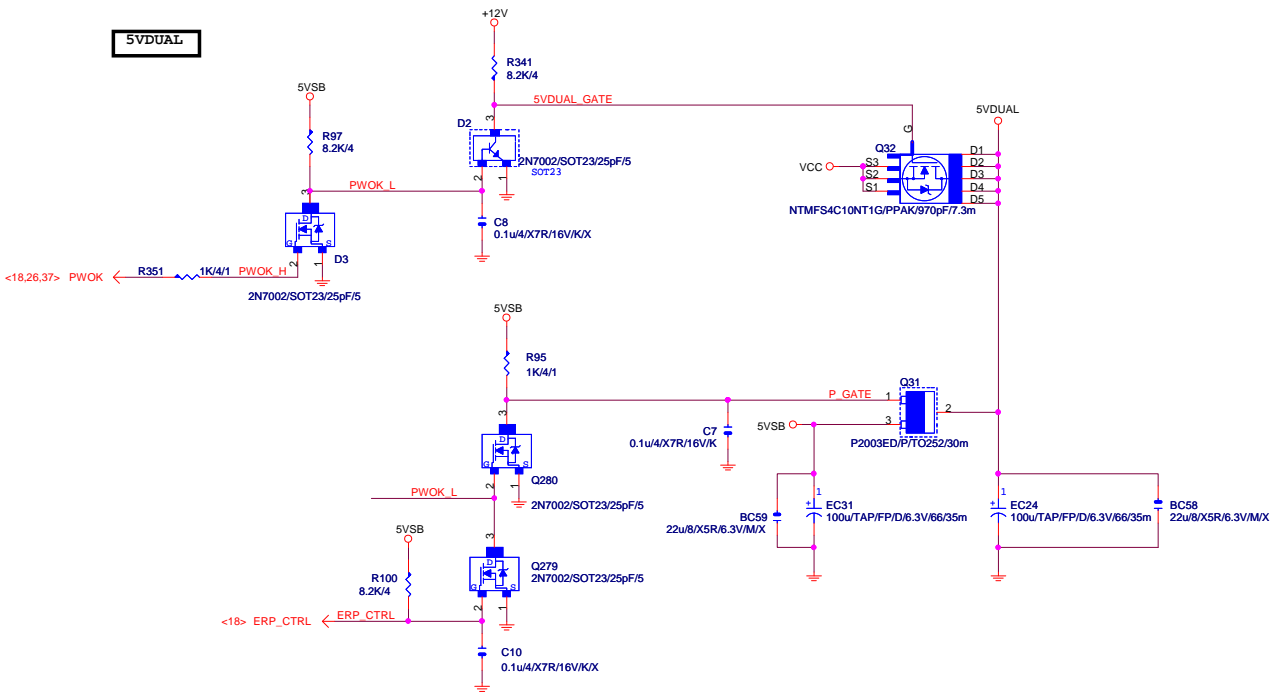
GIGABYTE™			
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VCORE MOS			
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VDDCR SOC S5

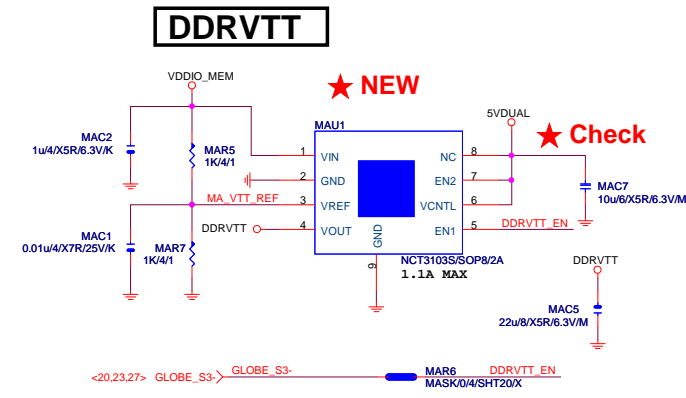
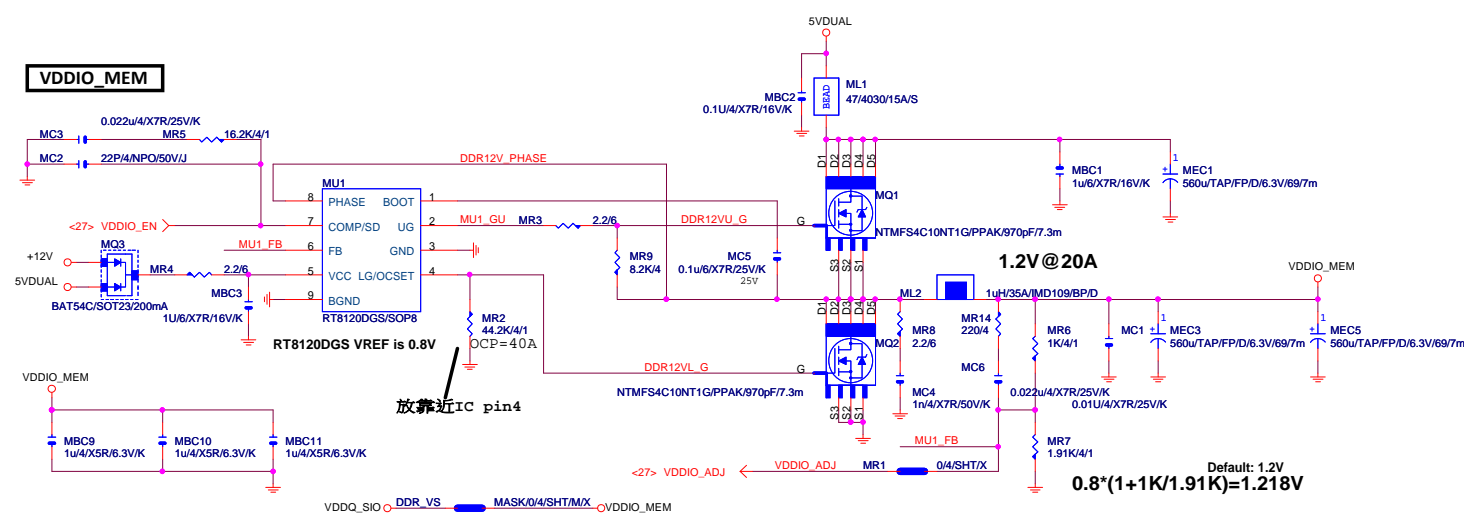
S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V), VDDCR_SOC_S5=0.775V.
If VCORE_SOC >= 0.775V (OR 0.85V), VDDCR_SOC_S5 will trace VCORE_SOC.





Vinafix.com

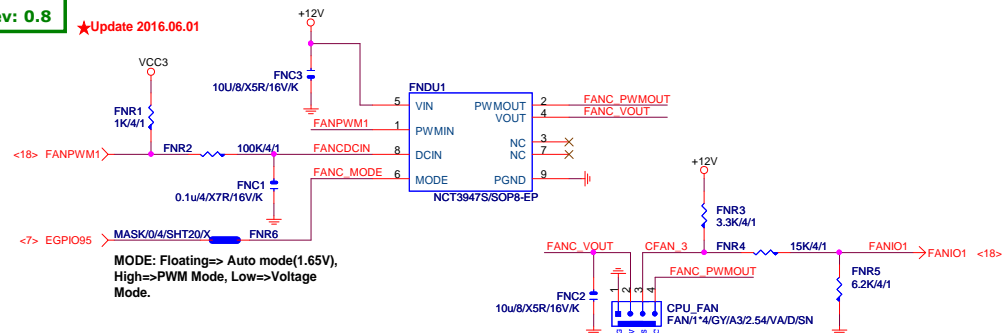
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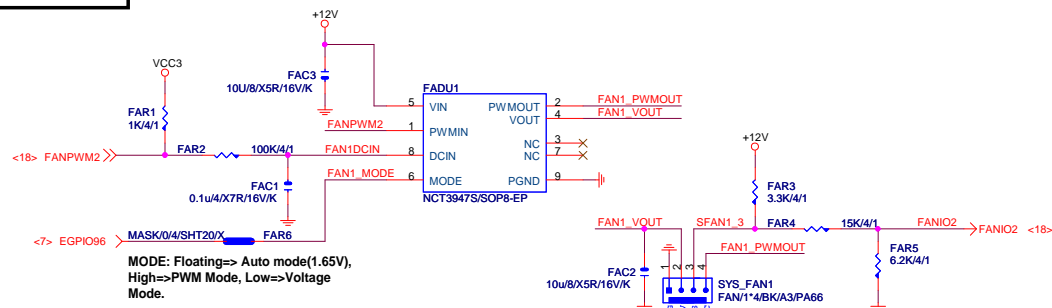
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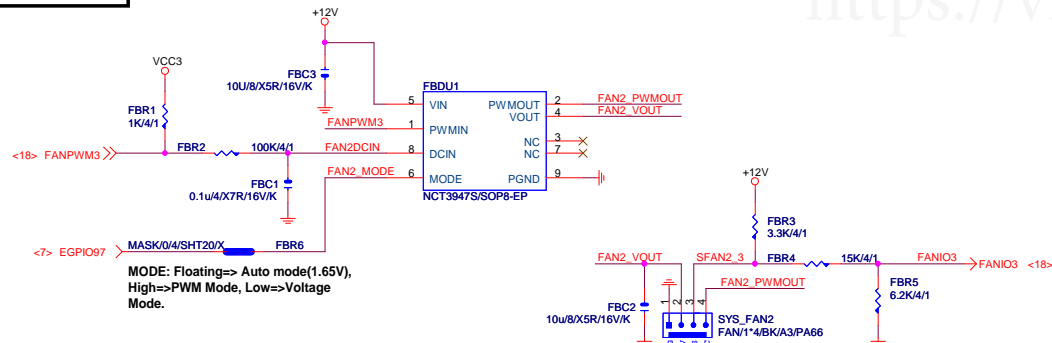
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SYSTEM FAN1



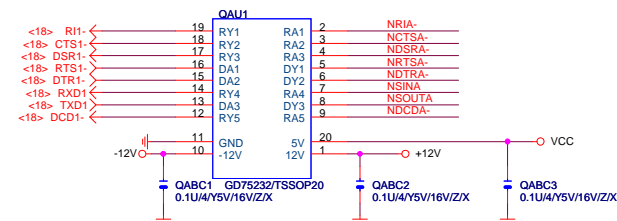
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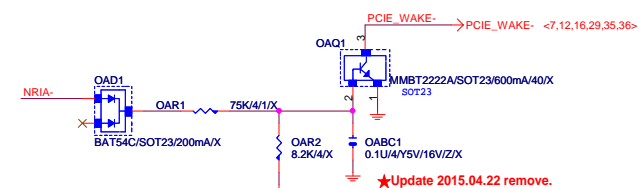
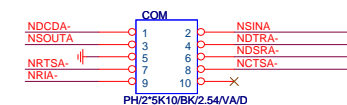
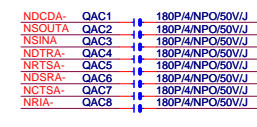
SYSTEM FAN3

LPT PORT

COM PORT COMA



R&D技術通報151 有使用PRINT PORT的
MODEL，需使用新料號:10HP2-118728-72R。(CHIP IT8728F/EX (GB) ITE/SMD
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。

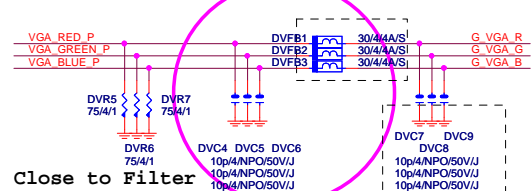
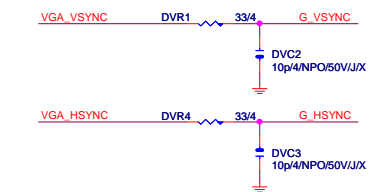
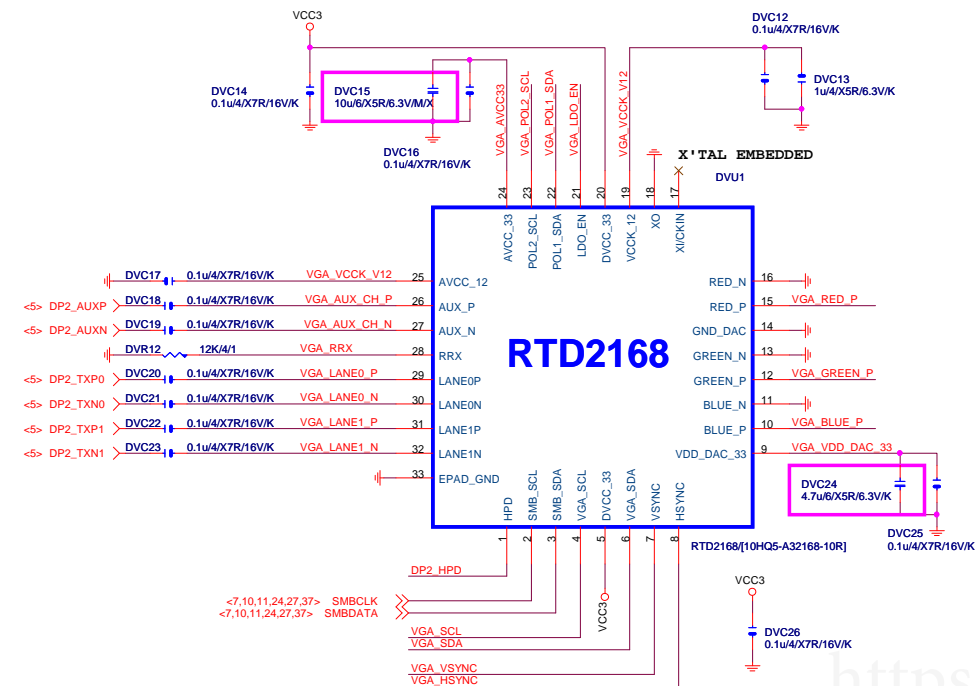


GIGABYTE™

Title FAN, LPT, COM

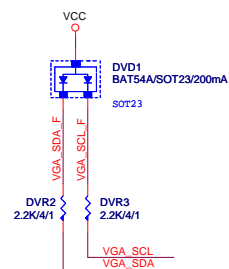
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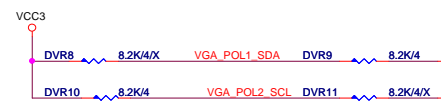


Close to Filter

FOR EMI



Power on latch



		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Embedded LDO

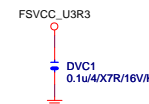
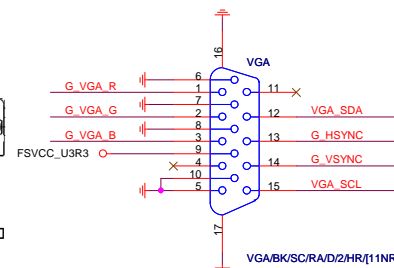
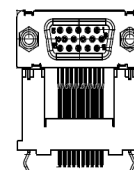


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

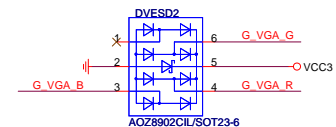
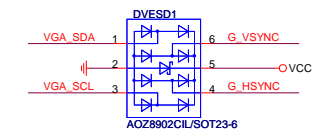
DP HPD

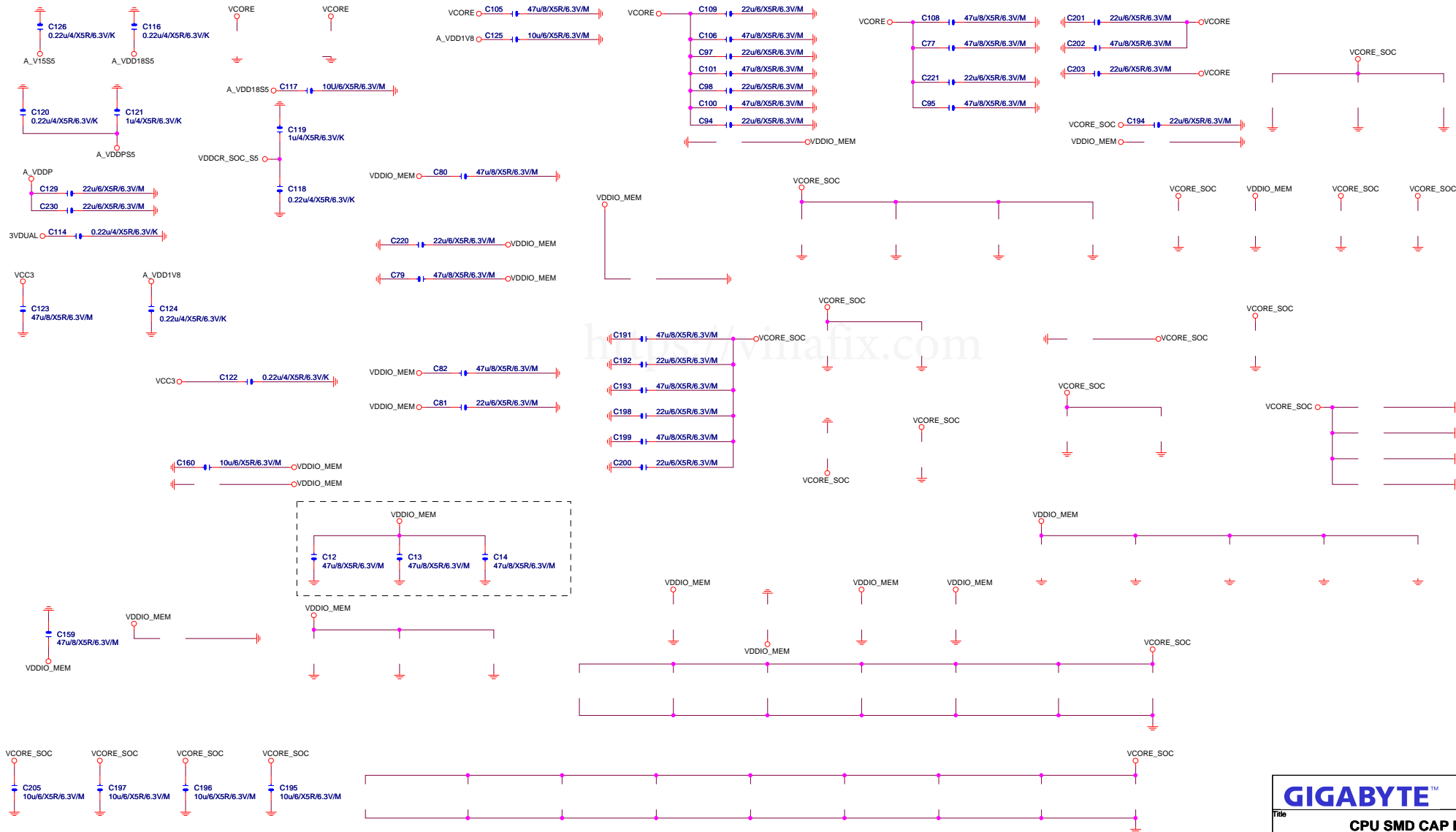
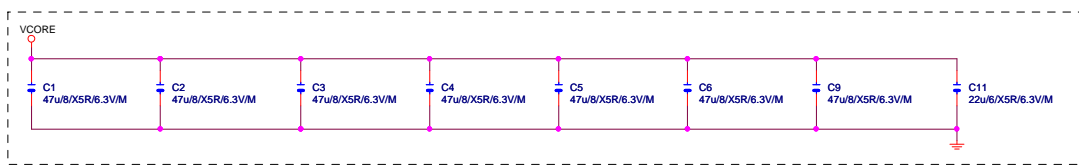


Gigabyte Technology

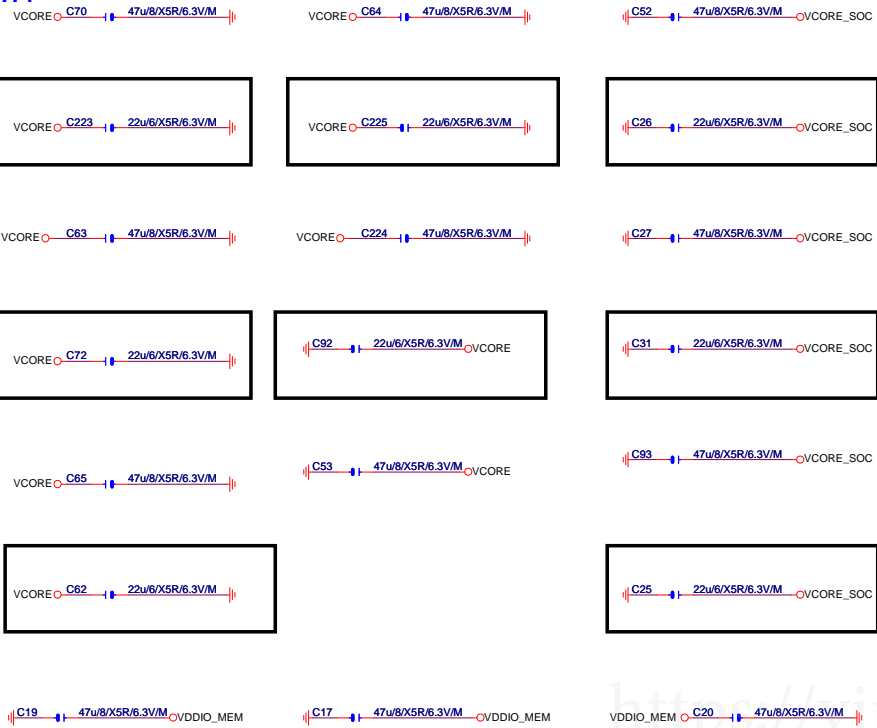


VGA ESD

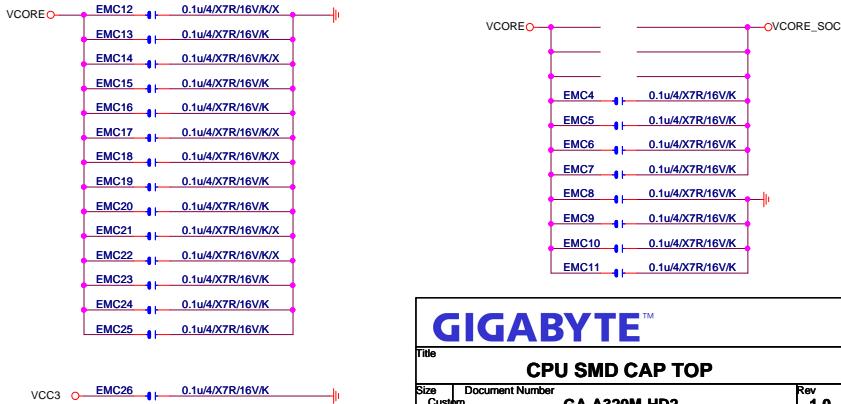




CPU TOP CAVITY



Cross Plane CAP



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Title

Size

Custom

Date

CPU SMD CAP TOP

Document Number

Tuesday, February 21, 2017

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Sheet

Rev

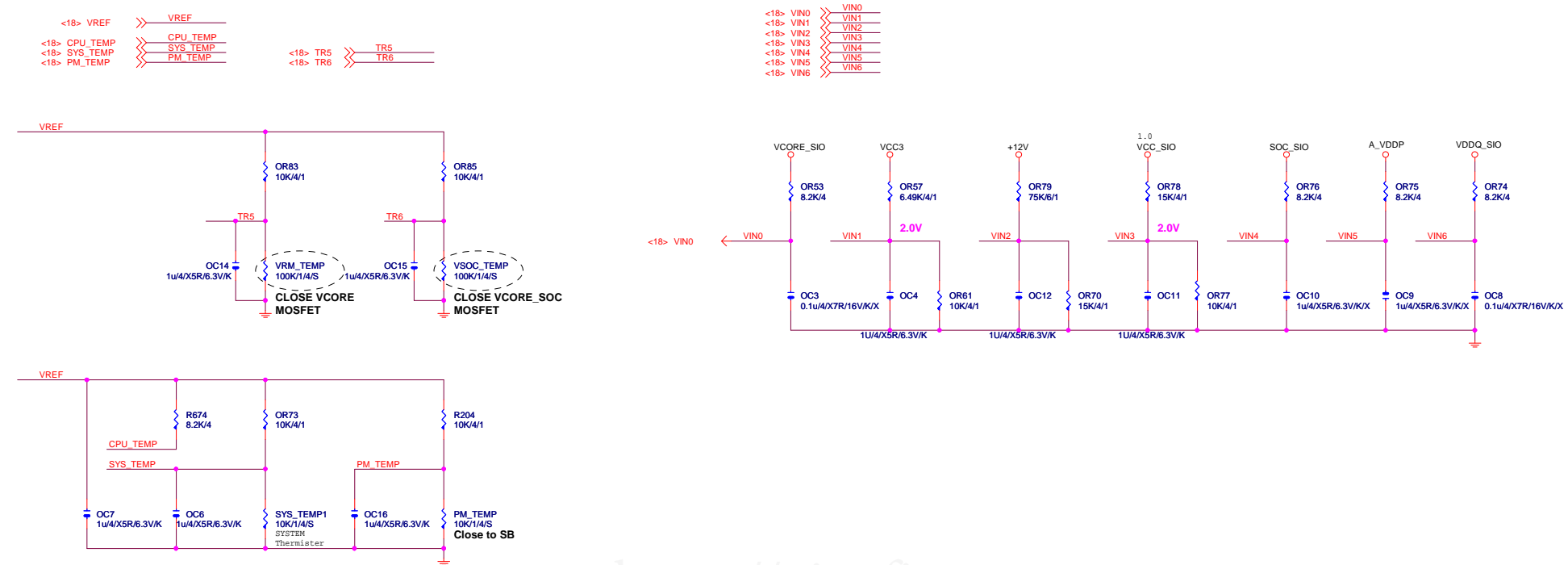
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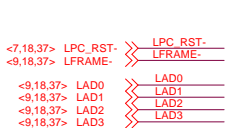
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38

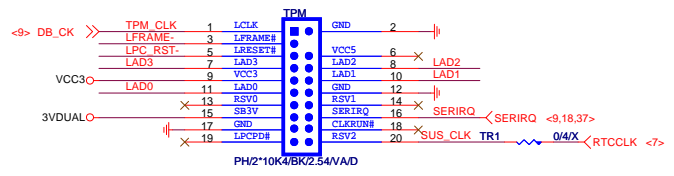
Hardware Monitor circuits



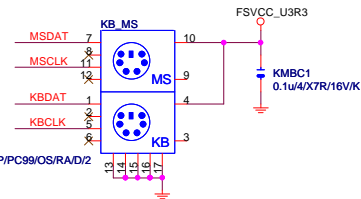
LPC Interface



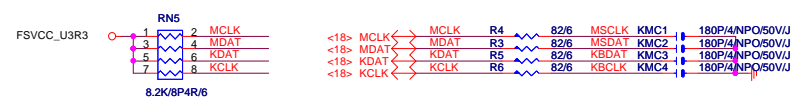
TPM Header

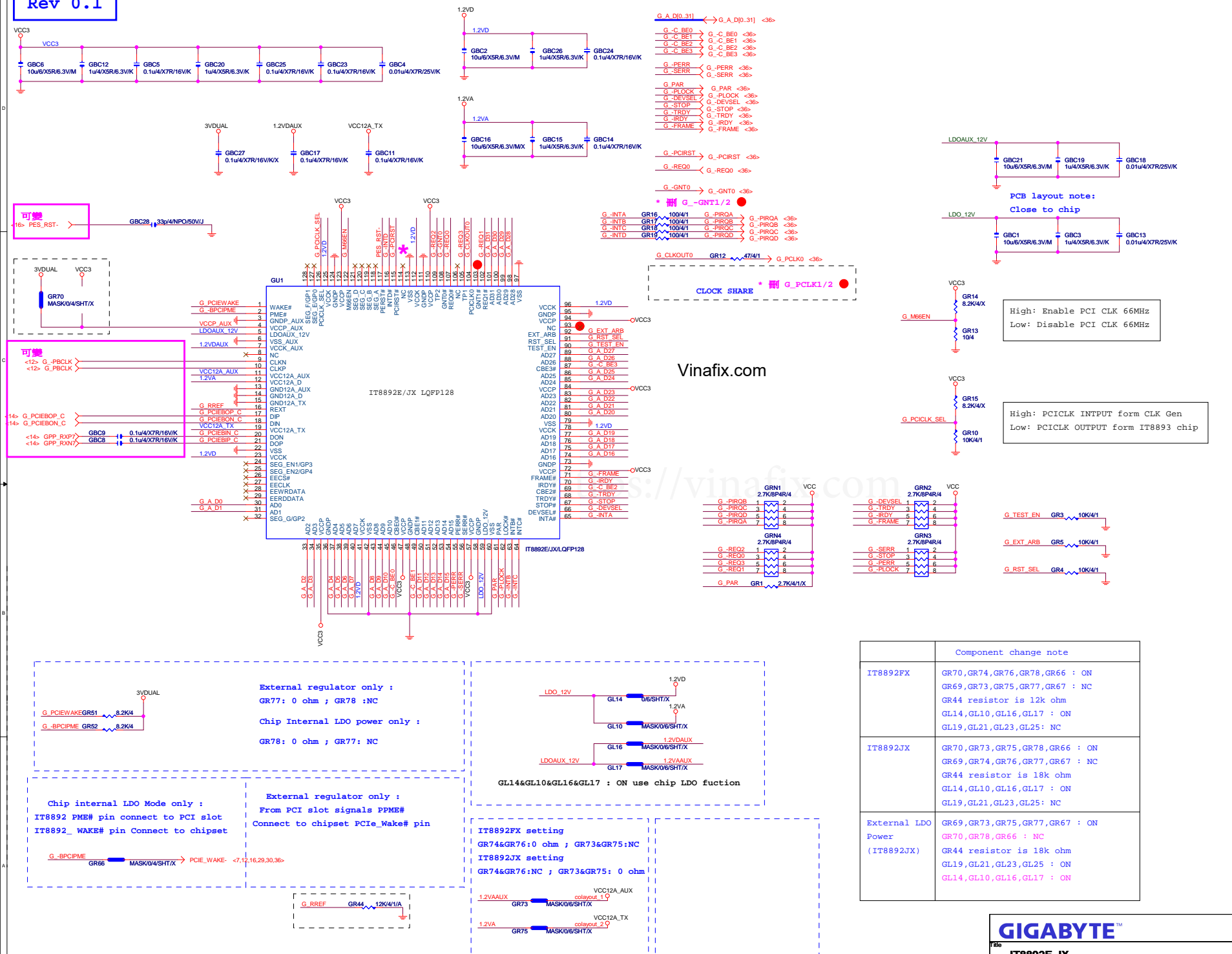


Debug Port Header



KB/MS & USB

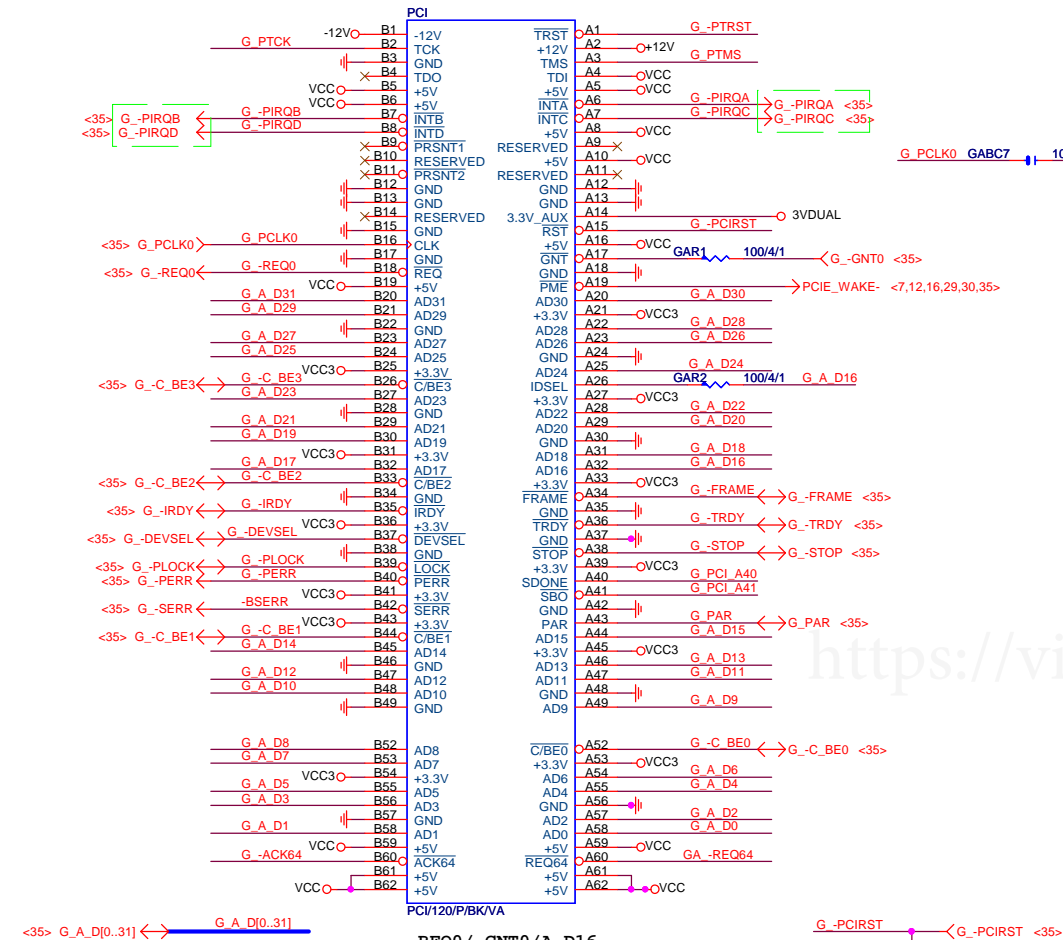




Rev 0.1

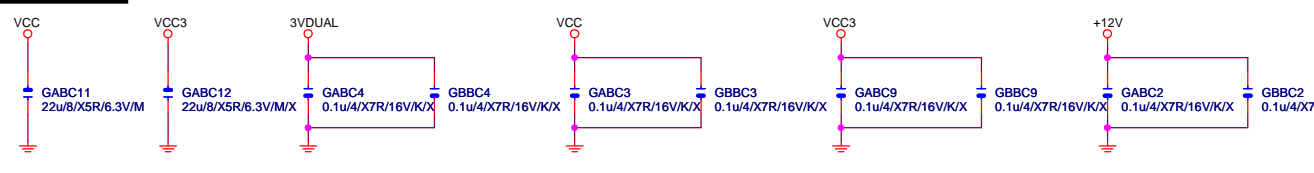
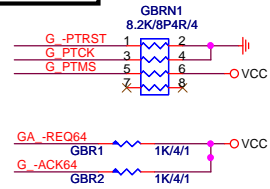
VCC3

PCI SLOT 1



PCI PU

PCI CAP

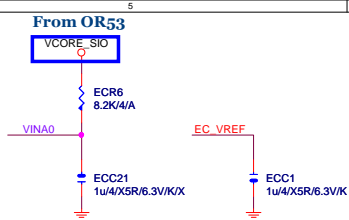


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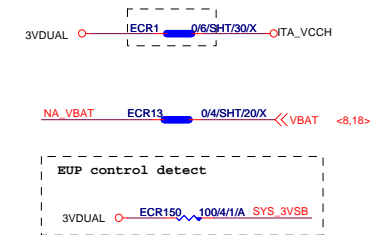
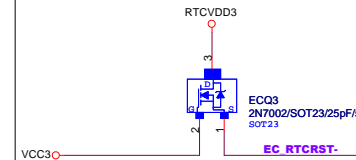
PCI SLOT 1&2

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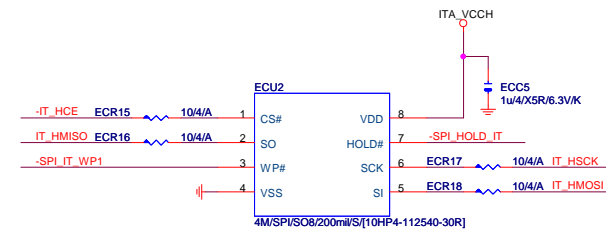
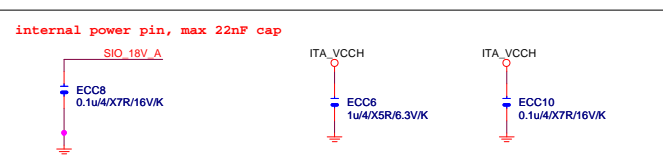
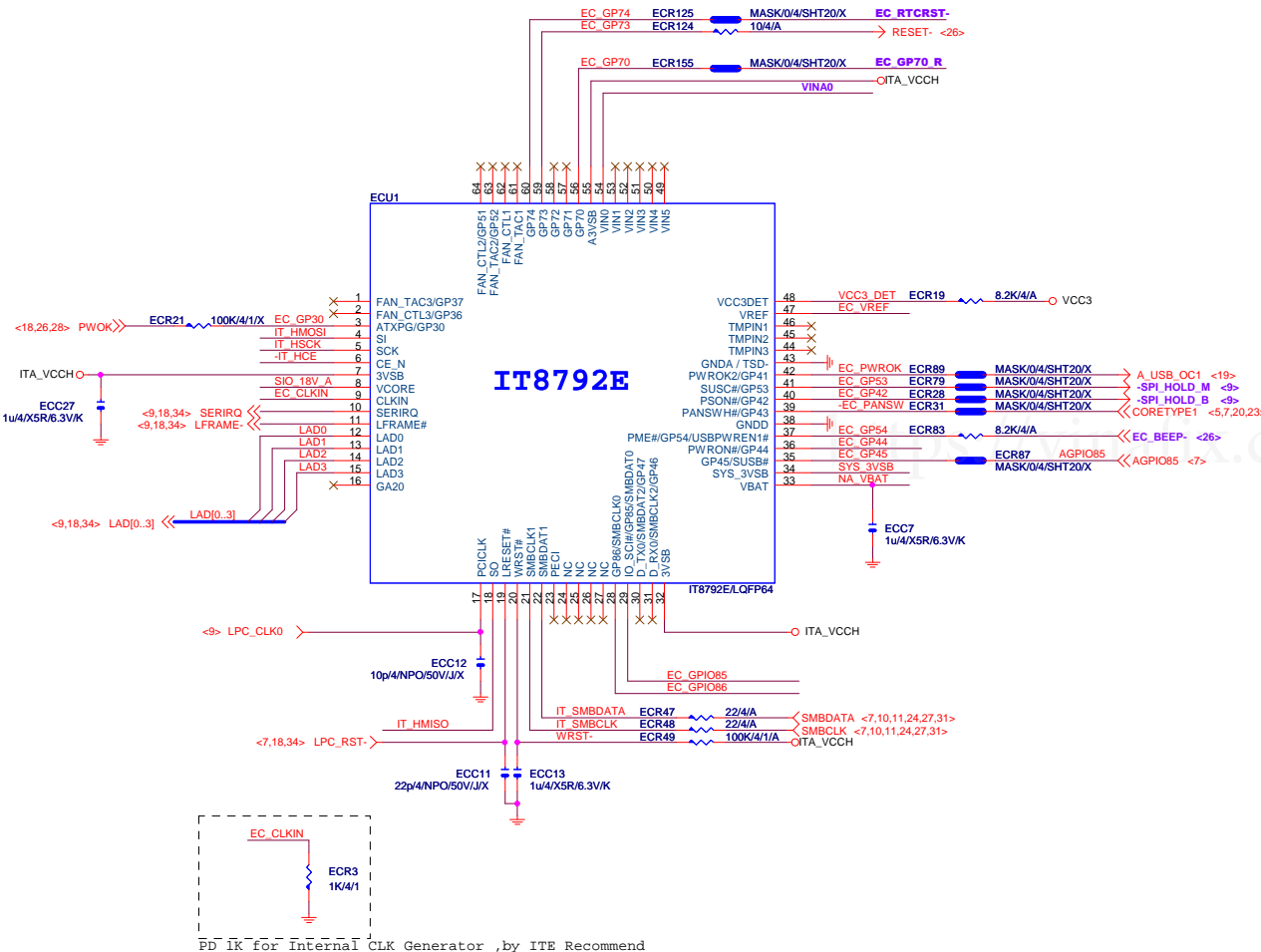
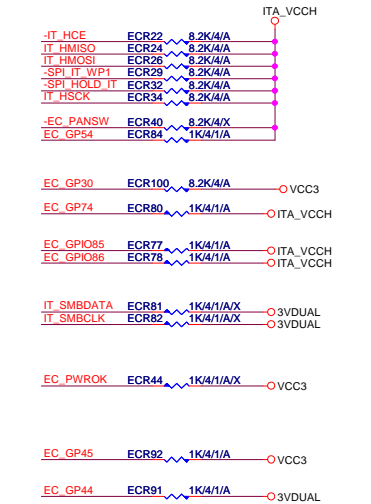
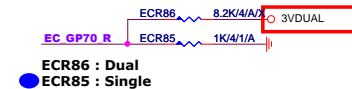
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Watch Dog



DUAL BIOS Strip



IT8686

